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Electrical Test Conditions & Considerations

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Electrical Test Conditions

The PCB industry is ever changing and adapting to new technology. OEM specifications and requirements have also advanced due to these technologies. With these advancements some things will still remain the same and some requirements will change. PCB manufactures are told what electrical test requirements are necessary for a given particular part via a FAB (Master) drawing. This is usually done during the "quoting" or "procurement" phase. When an OEM is deciding what requirements are required for a particular part regarding Electrical Test, some over precautions and/or disconnects may occur.

Electrical Test Parameters/Conditions

What are they? When a bare PCB undergoes Electrical Test the main goal is to determine if there are any "opens" or "shorts" in the design circuitry. Opens are defined as breaks in any given "net" or "circuit," while Shorts are defined as any non-desired connections between atypical or individual "nets" or "circuits." In the scope of IPC-9252A the main focus is in the resistance value "within" an individual circuit or the resistance between adjacent or other circuits. In Table 1 below the resistive thresholds are listed for the individual performance classes. In the case of "Indirect Isolation & Continuity Testing by Signature Comparison and Adjacency" these conditions will be explained later.

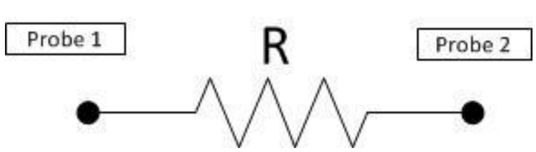
IPC 9252A Test Level C

Table 1

TEST LEVEL	A	B	C
Performance Class	1	2	3
Source Data	CAM, CAD	CAM, CAD	CAD[1]
TEST METHODS			
Resistive Continuity Testing	≤100Ω	≤50Ω	≤10Ω[4]
Resistive Isolation Testing	≥500kΩ	≥2MΩ	≥10MΩ
Indirect Isolation & Continuity Testing by Signature Comparison	Yes	Yes	AABUS
Adjacency (for isolation testing)[2,3]	Yes	Yes	AABUS

Now, from the table we must understand how the Grid Test Machines and Flying Probe Machines in Resistance Mode decipher what an "open" or "short" (or Continuity or Discontinuity in Flying Probe terms) are determined.

The Open or Continuity Fault (Performance Class C)



R value between 0 ohms to 10 ohms will **pass** electrical test.

R value 10.1 ohms or higher will **fail** electrical test.

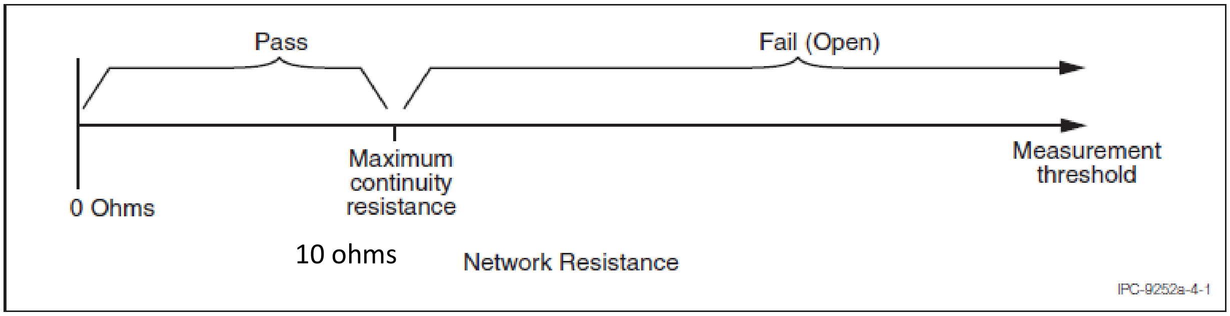
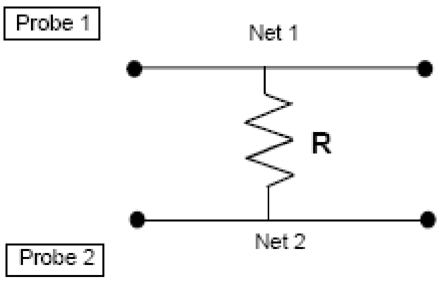


Figure 1:

The Isolation (short) or Discontinuity Fault (Performance Class C)

Level C also states that a resistive isolation test should be performed greater than 10 Meg Ohms, this means that any two networks that have an isolation resistance between 0.1 ohms and 10 Meg Ohms will fail electrical test for a short. If the isolation resistance is greater than 10.1 Meg Ohms the electrical test would pass.



R value between 0 ohms to 10 M ohms will **fail** electrical test.

R value 10.1 M ohms or higher will **pass** electrical test.

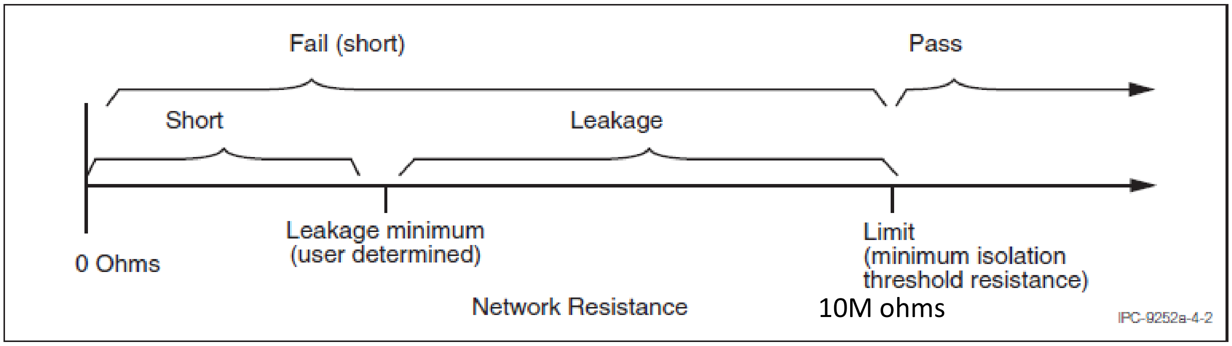


Figure2:

What happen to the test voltage?

The test voltage has been left open to the designers to be selected to a certain extent. IPC states that the Test Voltage shall be the Maximum Rated Voltage of the PCB if indicated on the Master Drawing or Procurement Document. If this is not stated and manual testing is used, the voltage applied shall be 200VDC minimum. If automated test equipment is used a voltage of 40VDC shall be used at a minimum. PCB's are used in a wide variety of applications. Every application may or may not have the need to specify a voltage requirement. If no voltage requirements are specified fabricators or service providers will use standard voltages chosen by them in accordance with the IPC minimum guidelines. The exception is IPC Class 3/A which is the IPC6012 exception for Aerospace and Military Avionics. This requirement is specific. The voltage shall be 250VDC, the Isolation shall be 100M Ohms and the Continuity shall be 10 Ohms. There are no exceptions to the Class 3/A rule.

Current Protection

Almost every electrical tester on the market has some sort of failsafe built into the measuring circuit that limits the amount of current reaching the PCB. Depending on the voltage range, different valued resistors may be used. These current limiting resistors will prevent the PCB from becoming damaged and the micro-fine shorts to be blown during the electrical test process.

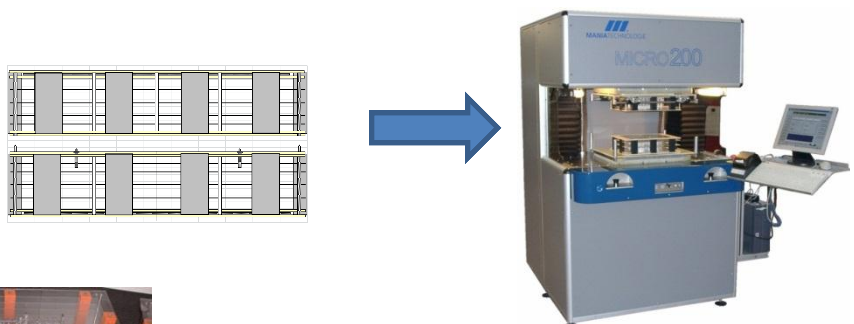
This is why a potential exists for escape when a circuit track is “dished-down,” severely etch-voided” or “splattered.” Electrical Test machines do not drive enough current to “burn” the connection. Unfortunately this type of condition usually manifests itself during the assembly process post wave-solder or thermal stress.

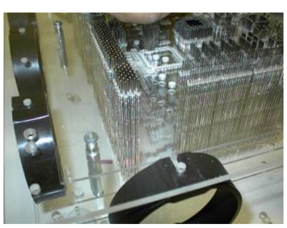
Caution:

- **Electrical testing parameters that allow high productivity could also allow higher defect rates**
- **Electrical test voltage set to low may allow readings to be out of specifications**

With today’s technology there is a phenomenon that is built into the PCB that can cause erroneous readings with regard to Isolation Testing. This is caused by cores that are built into the PCB that exhibit buried or intentional capacitance. Although desired in the build by the design team it can cause trouble during Electrical Test. If the Electrical Test facility is not made aware of this type of build, false Isolation (shorts) will be reported and cause unnecessary non-conformance or scrap. Electrical Test Machines can combat this anomaly if the department is notified of this design characteristic. Conversely, another oversight that comes up is the excessive length of copper in a single net or node. The desired performance class has limitations in the Ohm value that can be reported to keep the node or net conforming. In the case of attenuation or “heater” circuits the length of the net can far exceed the Ohm value required by the performance class. This can cause delays, MRB evaluation or possible incorrect disposition of the product. These atypical design variables must be conveyed to the manufacturer up front in the PO or Master Drawing to avoid unnecessary delays or scrap.

How does a universal grid tester test a PCB using these parameters?





A “Jig” or “Fixture” is required to transfer the voltage/current from the base of the machine to the node on the PCB. Typically this causes a minimal amount of connection resistance between the base of the machine and the fixture. Similarly there will be a small connection resistance from the fixture to the nodes of the PCB’s. The majority of universal grid machines are able to null these connection resistances through their calibration process. The lowest resistance that currently can be reliably measured on a grid tester is 5 ohms. The maximum test voltage that can be used on a solid state universal grid tester is 250V. The maximum isolation resistance that can be measured reliably is 100 M ohms.

Typically a grid tester will perform some sort of pattern scan once for continuity and once for the isolation test. This scan and test will allow for a full parametric test. This means that every net will be checked against each other for isolation.

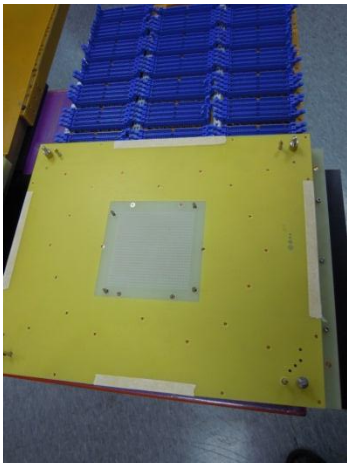
There are several different pitch levels of universal grid testers 100mil, 80mil, 70mil, 50mil, and 25mil.

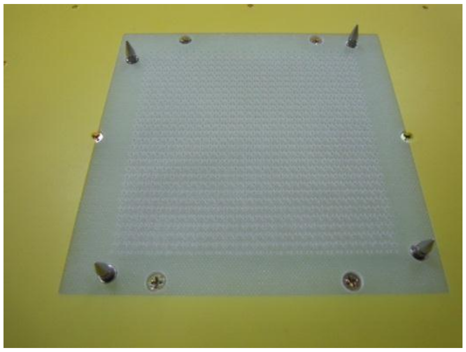
Universal grid testers offer one of the most comprehensive tests because you are always covering the completed PCB as long as the nodes have active test points on them. All defects such as layer to layer shorts will be detected.

How does a dedicated tester test a PCB using these parameters?

Dedicated testers operate on the very same principals as the universal grid testers. The major difference between the two machines is that the dedicated machines do not have a universal grid to work with. Each test point is hard wired back to some sort of connection module. This hard wired system allows for two major advantages, the first is it removes the limitation of a

universal tester about having to locate a universal grid location for each pin. This will remove friction on the test pin which allows for better reliability testing performances in HDI product.
The second main advantage is that the standard solid state switching technology can be replaced by relay switches which allow for higher voltages to be applied. This can be beneficial for high reliability requirements.





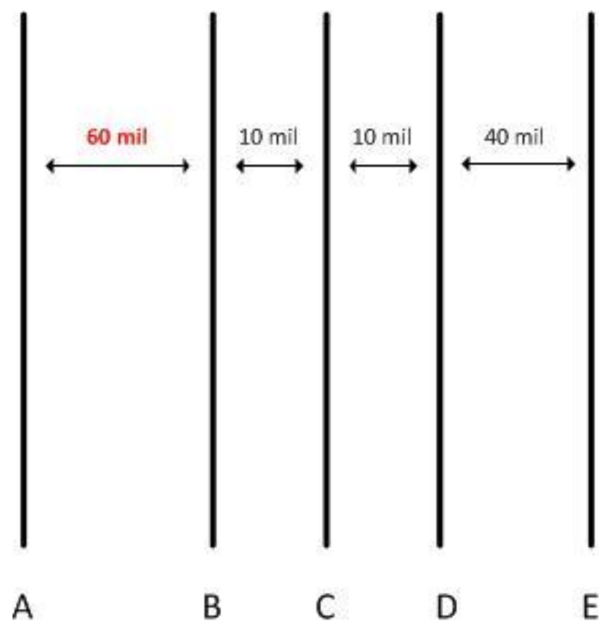
Dedicated testers offer the same comprehensive test as the universal grid machines.

How does a Flying Probe tester test a PCB using these parameters?


A Flying Probe tester has one of the more complex test methods because there are various ways that the machine can be setup to test a PCB. IPC 9252A defines these test methods in two categories (Direct and Indirect).

Direct test method:
This test method for continuity test will apply the specified voltage and current to each net and measure the applicable end point nodes for the resistance value. If the resistance value is below the set threshold a pass will be recorded.
Direct isolation test will **not** test each net against every other net for shorts, it will use some sort of adjacency methodology (See Figure line of site). The voltage and current is applied to one net and the other adjacent nets are measured for leakage current.

Figure3 of Line of Site Adjacency



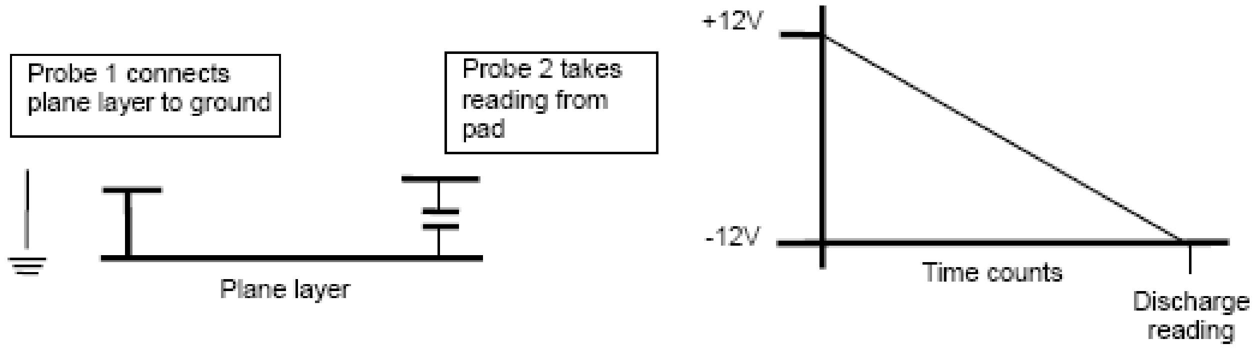
This method tests nets that lie within the line of sight of each other on the same layer. The nets must also lie within a fixed horizontal space usually 50 mils. The figure shows five traces that are side by side and are identified with A,B,C,D,& E. Net C in this Figure would be tested against nets B & D. Nets A & E would not be tested against net C because there are not adjacent to each other. Net A would not be checked against net B because it falls outside the horizontal distance window of 50 mils. Net D would be checked against net E because it is next to D and the horizontal distance is less than the 50 mils.

Indirect test method

This method uses something called signature comparison. Each net is **not** checked individually for continuity or isolation, instead each net is compared against a master set of values. In this method the Flying Probe has a netlist of the PCB in its required input format. This can be direct IPC or another format. For the Indirect Testing by Signature Comparison the first board will receive a more advanced test than subsequent boards. Indirect or Capacitance test will have the machine place a probe on the "reference" point that is a plane layer. The other probes will then process all the other test points in the PCB as "readers" or "antennae." These values will then be placed in a temporary file. The machine will then do a full point-to-point Continuity test in resistive mode checking all nodes against the set resistance threshold. Any violations will be reported as "Opens" and that net will be flagged in the temporary master as suspect. When the Continuity test is completed the Isolation test will be initiated using the Isolation threshold. Keep in mind the Adjacency window will be used as explained above. Any nets found in violation will be reported as "Shorted" and the nets will be flagged as suspect in the capacitance signature. The capacitance file will now be written as the master but in this case with possible suspect nets.

The second board is now tested. The machine will again do the signature (capacitance) gather but this time it will compare the readings to the previous master. All nets that report within the master capacitance values will be flagged as good and will not require any resistance verification. Any nets that violate the master will automatically be flagged for resistance verification. Also on the second board if any nets were flagged as incorrect from the first board (that may have actually failed) they will automatically receive resistive Continuity and Isolation tests. These are to validate the nets against the original netlist. If these possible nets are now validated the capacitance master is then updated.

The third board is now tested. The machine again performs the signature (capacitance) gather. This time the master has all good values and if this board exhibits capacitive readings all within the master values it will pass with no resistive retests.



Limitations with Indirect Test Method

Figure4: Capacitance Measurements (Discharge Gather)

A limitation exists with the indirect method when it comes to the Electrical Test Certificate of Compliance.
Most OEMs are complacent to see electrical test parameters noted on the C of C. With the Indirect method these parameter on the C of C are not possible as only nets RETESTED after the capacitive discharge gather will actually receive the Class I, II or III direct voltage, Isolation and Continuity parameters. Only the first board tested will receive these requisites. This is why you see in Table 1 under performance class C that Indirect Testing and Adjacency are labeled AABUS. This means that an agreement between User (OEM) and Supplier (Manufacturer) must be agreed upon during the quoting or contract realization phase. At the time of this writing Indirect Testing or Flying Probe test on any Class 3/A per IPC6012C Class 3/A Exception for Aerospace and Military Avionics are not allowed.

Conclusion:
When testing PCBs it can be quite confusing as to what method to use, parameters are necessary for the Performance Class and what cost to associate in the build to way against the long term reliability of the product. Design anomalies and capacitive cores can further cause stress in the once thought streamlined process. Understanding how the machines and methods test the product up front may alleviate delays and unnecessary waste in what otherwise would have been conforming product and delivered on-time. From the OEM side the better understanding of how the methods and parameters work against the product can better inform the manufacturer of possible anomalies in the final inspection process. If these are communicated up front, unnecessary delays can be omitted.

Thank you for attending….