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Effect of Gold Content on the Reliability of SnAgCu Solder Joints

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Abstract
Electroplated Ni/Au over Cu is a popular metallization for PCB finish as well as for component leads, especially wire-bondable high frequency packages, where the gold thickness requirement for wire bonding is high. The general understanding is that less than 3 wt% of Au is acceptable in SnPb solder joints. However, little is known about the effect of Au content on the reliability of SnAgCu solder joints. The purpose of this study is to determine the acceptable level of Au in SAC305 solder joints. Three different package platforms with different Au thicknesses were assembled on boards with two different Au thicknesses using a standard surface mount assembly line in a realistic production environment. The assembled boards were divided into three groups: as-built, isothermally aged at 125°C for 30 days, and isothermally aged at 125°C for 56 days. All boards were then subjected to accelerated mechanical reliability tests including random vibration and drop testing. The results show that solder joints with over 10 wt% Au are unacceptable. If Cu is available to dissolve in the solder joint, then an Au content under 5 wt% will not significantly degrade the reliability of the solder joint. When Ni layers are present on both the board and component sides of the interface, this limits the ability of Cu to dissolve into the solder joint and hence an Au content under 3 wt% is acceptable. The failure mechanism for solder joints with high Au content is fractures through the $AuSn_4$ IMC. Our comprehensive long-term reliability study did not confirm the finding by Ho et al. (2002) that the weak interface between (Au, Ni)Sn_4 and Ni_3Sn_4 results in brittle interfacial failure. Additional findings confirmed the danger of placing parts near high stress areas and that a high level of voiding reduced reliability.

Introduction
Electroplated Ni/Au over Cu is a popular metallization for PCB surface finish as well as for component leads. The Ni layer functions as a diffusion barrier layer. The Au layer is used to 1) protect the Ni layer from oxidation and corrosion, 2) to enhance the soldering wettability, and 3) to improve wire bondability in some applications.

During the soldering process, Au dissolves into molten solder very quickly. It has been reported that molten Sn can erode a nominally 25 µm thick layer of Au in 10 seconds at 235°C (Humpston and Jacobson, 2004) and the dissolution rate of Au in Sn40Pb (60 wt% Sn and 40 wt% Pb) solder is as high as 4.2 µm per second at 252°C (Bader, 1969 & 1980). At such a rapid dissolution rate, all Au in a PCB and component lead, which has typically less than 0.8 µm of Au, will be dissolved in a typical lead-free reflow profile where the time above liquidus is generally 30 to 90 seconds. When the solder joint solidifies, a brittle $AuSn_4$ or (Au, Ni)Sn_4 IMC is formed in the solder joint. The presence of brittle $AuSn_4$ or (Au, Ni)Sn_4 IMC in the solder raises concerns about reliability.

The current understanding about the failure mechanism of "Au embrittlement" is as follows: when the solder joint solidifies during the soldering process, brittle $AuSn_4$ or (Au, Ni)Sn_4 IMC is formed in the bulk solder joint. After aging, the $AuSn_4$ migrates to the Ni interface and forms a continuous layer of (Au, Ni)Sn_4 IMC over the Ni_3Sn_4 IMC layer. The weak interface between (Au, Ni)Sn_4 and Ni_3Sn_4 results in brittle interfacial failure (Ho et al., 2002). The driving force for the migration of $AuSn_4$ is a reduction of energy by mixing. Gold seeks Ni so that $AuSn_4$ becomes a Ni-saturated (Au, Ni)Sn_4 compound (Ho, et al., 2002). It has been reported that the thickness of the Ni layer has a significant effect in Au embrittlement as well. Alam et al. (2005 & 2006) found that a thin layer of Ni facilitates the diffusion of Cu into the (Au, Ni)Sn_4-solder interface and changes the (Au, Ni)Sn_4 layer to a (Au, Cu, Ni)$_6Sn_5$ layer. They explained that the elimination of the brittle layer of (Au, Ni)Sn_4 IMC over Ni_3Sn_4 layer prevents cracks from propagating along the interface between (Au, Ni)Sn_4 and Ni_3Sn_4. Though a thin Ni layer has this benefit, in practice, a thin Ni layer may limit PCB shelf life and solderability.

Less than 3 wt% of Au is considered to be acceptable in SnPb solder joints. A comprehensive study was conducted by Glazer et al. (1992). They investigated the effect of Au content on the long-term reliability in the defined service environment of SnPb solder joints between a plastic QFP component and a PCB with Ni/Au finish and concluded that 3.0 wt% of Au is acceptable. However, little is known about the effect of Au content on the long-term reliability of SnAgCu solder joints. The objective of this study is to fill this void.

There are two differences between the eutectic SnPb solder and the SnAgCu solder on the dissolution of Au and their effect on the reliability of solder joints. One is the high-Sn content effect. The Sn content in Sn3.0Ag0.5Cu solder is 96.5 wt% and that in eutectic SnPb solder is 63 wt%. Intuitively, a solder with higher Sn content should be able to take more Au to form $AuSn_4$ IMC. Chang, et al. (2006) also found that the migration kinetics of the $AuSn_4$ to the solder/pad interface during

thermal aging in high-Sn solders was slower compared to that in eutectic PbSn. The other is the Cu effect in the SnAgCu solder. Shiau, et al. (2002) showed that 0.5 wt% of Cu can reduce the Ni consumption rate in solder joints with a Ni/Au surface finish.

In this paper, we report on a comprehensive study regarding the effect of Au content on the long-term reliability of SnAgCu solder joints in three different package platforms on PCBs with a Ni/Au surface finish. First, the Au content in the final solder joint is calculated based on the measured solder paste volume and the measured Au thickness in the PCB surface finish and/or the component surface finish. The assembled boards were divided into three groups: one without any thermal treatment, one isothermally aged at 125°C for 30 days and the third group aged at 125°C for 56 days. All three groups were subjected to the long-term mechanical reliability testing including random vibration and mechanical shock. The reliability test plan was based on Agilent's typical industrial instrument operation environment. The reliability data are reported. Furthermore, the failure locations and mechanisms are presented.

Methodology

Component, Test Vehicle, and Assembly Process

The test vehicle is shown in Figure 1. The PCB employed has six-layers and is made of Nelco© N4000-12. The board finish is electrolytic Au over Ni. There are two different Au thicknesses: a flash Au finish with 0.08 ~ 0.38 µm Au over 5 µm Ni and a thick Au finish with 2 ~ 2.54 µm Au over 5 µm Ni. Five types of components were assembled on the test vehicle. All components were daisy-chained. The package information is summarized in Table 1. There are nine QFN5 packages, nine QFN6 packages, nine TOPS packages, six FP I packages, and six FP II packages per board. All components have underbelly pads.

The assembly process was done using a standard surface mount assembly line in a realistic production environment. The solder paste used is Sn3.0Ag0.5Cu (SAC305) Type 3 with no-clean flux and metal content of 88% by weight. The stencil used is electroformed Nickel, laser cut with the foil thickness of 0.1 mm (4 mils) and 1:1 aperture to pad ratio. The volume, area, and height of solder paste on each pad of each board were measured by a solder paste inspection system. The reflow process was done in nitrogen and the reflow profile is shown in Figure 2. After assembly, the resistance of every daisy-chain was measured and documented. All solder joints were inspected using 2D X-ray. Any defects related to the assembly such as missing wire bonds in the component, insufficient solder and bent lead were documented.

Table 1. Summary of Packages

Package Type	Number of packages per board	Package Size and Type	Lead Material	Lead Finish
QFN5	9	5 mm x 5 mm Quad flat no lead	Cu	Matte Sn
QFN6	9	6 mm x 6 mm Quad flat no lead	Cu	Matte Sn
TOPS	9	10 mm x 10 mm RF laminate, open cavity, no lead	Cu	0.28 ~ 0.46 µm Au over 3.8 ~8.5 µm Ni
FP I	6	6.4 mm x 6.4 mm Ceramic, open cavity, flat leads	Kovar	1~2 µm Au over 1~ 5 µm Ni
FP II	6	10.2 mm x 9.7 mm Ceramic, open cavity, flat leads	Kovar	1~2 µm Au over 1~ 5 µm Ni

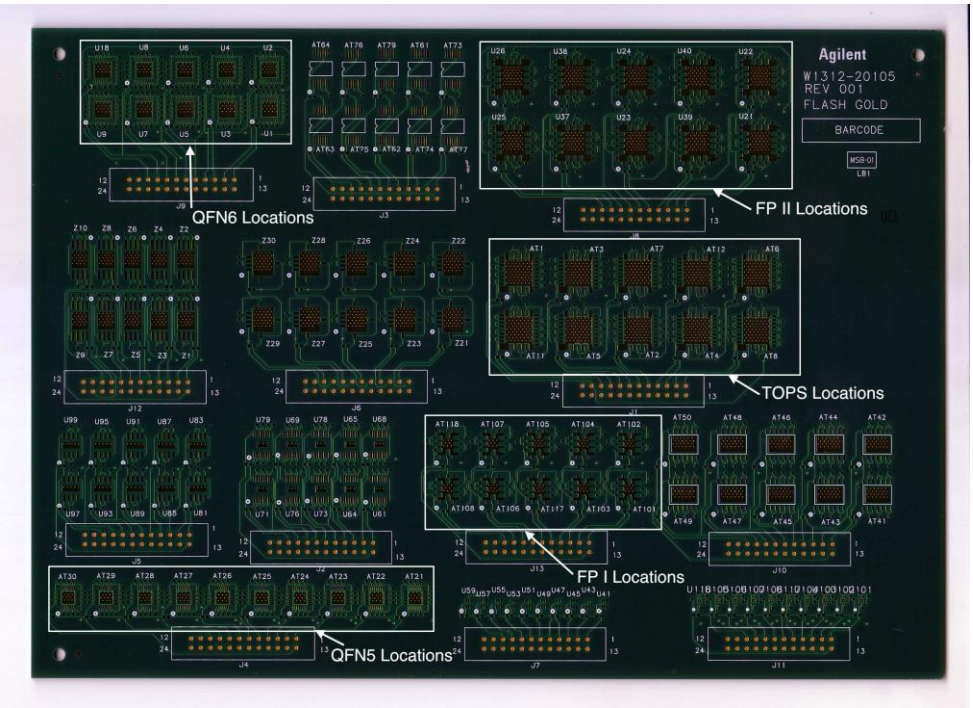
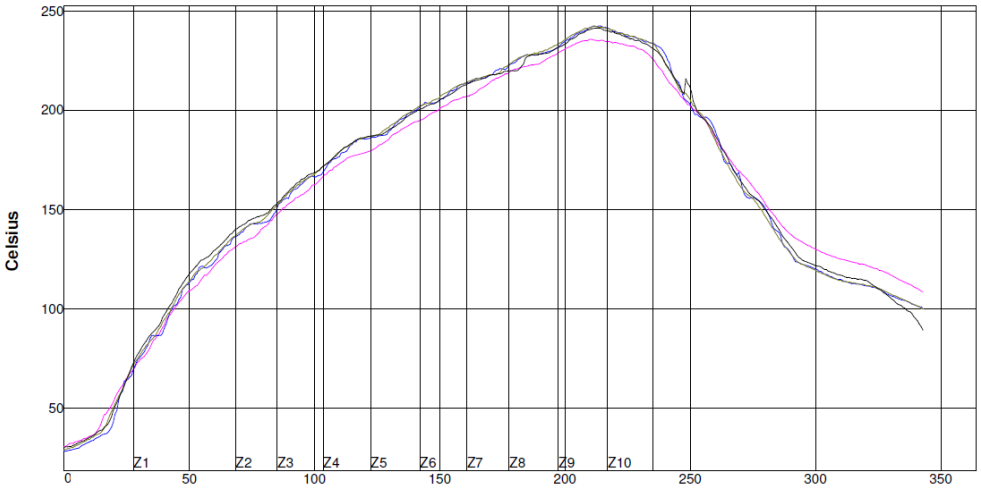


Figure 1. Test Vehicle

Setpoints (Celsius)										
Zone	1	2	3	4	5	6	7	8	9	10
Top	150.0	165.0	170.0	200.0	220.0	230.0	240.0	250.0	265.0	230.0
Bottom	150.0	165.0	170.0	200.0	220.0	230.0	240.0	250.0	265.0	230.0
Conveyor Speed (inch/min):	36.01									



PWI= 81%	Max Rising Slope		Max Falling Slope		Soak Time 150-217C		Reflow Time /217C		Peak Temp	
U22 PIN10	2.00	25%	-1.77	49%	87.09	81%	65.71	12%	236.12	-54%
AT1 PIN23	2.51	57%	-2.12	26%	84.63	64%	73.78	41%	242.62	18%
AT1 GND	2.33	45%	-2.19	20%	84.79	65%	75.15	46%	242.83	20%
U18 GND	2.47	54%	-2.42	5%	86.34	76%	74.67	44%	241.56	6%
Delta	0.51		0.65		2.46		9.44		6.71	

Figure 2. Reflow profile used in this study

Reliability Testing

The assembled PCBs were randomly divided into three groups as shown in Table 2. The boards in Group 1 were not subjected to thermal aging. The boards in Group 2 were subjected to isothermal aging at 125°C for 30 days. The boards in Group 3 were subjected to isothermal aging at 125°C for 56 days. The isothermal aging at 125°C for 0 hrs, 30 days, and 56 days was to simulate reliability life of 0, 7 years, and 14 years when devices operate at 60°C.

All boards were subjected to mechanical reliability testing. Each mechanical reliability test cycle includes 1) random vibration at power spectral density (PSD) of 0.002868 g^2/hz, 5 Hz ~ 120 Hz for 50 minutes, and 2) mechanical shock at 250G, 2.3 msec duration for 10 drops. Random vibration is chosen instead of sinusoidal vibration because it has been shown that random vibration more closely represents the true environment (Steinberg, 1988). In the vibration testing, it is important to select two key parameters: frequency range and PSD level because the reliability of solder joints on a board is mainly determined by these two parameters. It is advised that the test frequency range should include the natural frequency of the test board because at this frequency the board will experience the highest displacement, which generates highest stresses on solder joints. The natural frequency of the test vehicle was measured at 61 Hz. The acceleration level of this random test is 0.57G root mean square (RMS), which is calculated by the square root of the area under the random vibration curve, or $\sqrt{0.002868G^2/Hz \times (120-5)Hz}$. The acceleration level of 0.57 Grms is about 2 times of the typical vibration profile (in the range between 0.20 and 0.35 Grms) that products experience in transport as specified in a report by L.A.B. Equipment (2006).

Equation 1 is used to estimate the vibration fatigue life (Steinberg, 1988)

$$T_1 G_1^b = T_2 G_2^b \quad (1)$$

where T is life time, G is the acceleration in RMS, and b is the fatigue exponent. In this study we assume the fatigue exponent b is equal to 3 for leadless or flat lead parts at a printed circuit assembly level, and because we have a PSD level that is 2 times the expected real-life transportation level. Note that the vibration-fatigue exponent for aluminum leads has been specified as 6.4 (Steinberg, 1988). Military standard MIL-STD-810G specifies 7.5, and mentions a range of 5 to 8 for fatigue exponent (MIL-STD-810G). Thus, our estimation is more conservative. The vibration for 500 minutes in this study simulates the real vibration life of

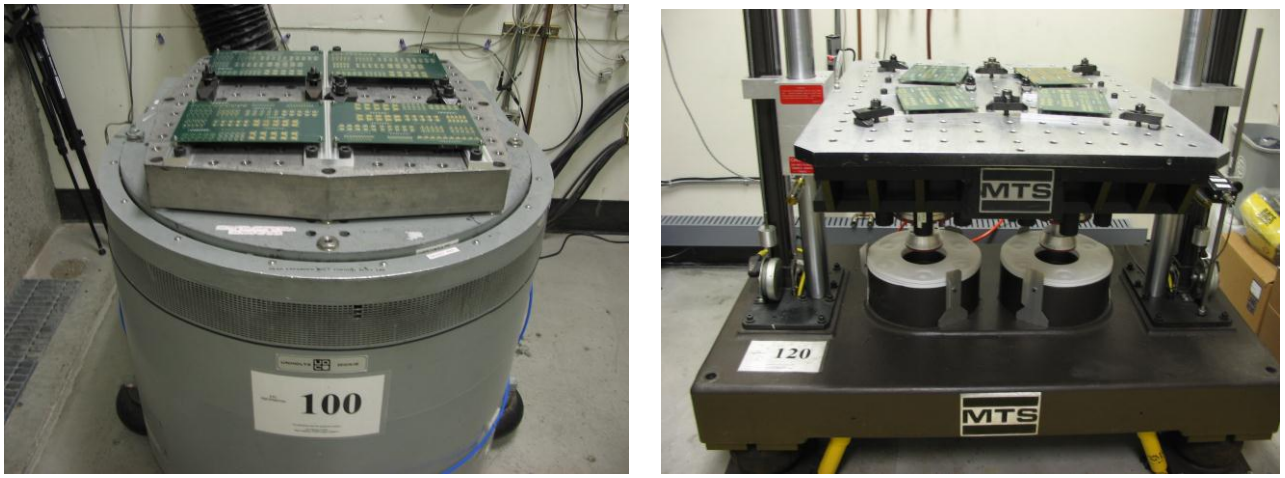
$$T_1 = T_2 (\frac{G_2}{G_1})^b == 500 \times 2^3 = 4{,}000 \text{ minutes } = 67 \text{ hours}$$

The setups for the random vibration and the drop tests are shown in Figure 3. The board was placed in a horizontal orientation with components facing in a downward direction, which results in maximum board deflection. All boards were subjected to 10 cycles of random vibration, or 500 minutes total, and 100 drops.

The resistance of each daisy-chain was measured by an Agilent 34970A data logger with three 34901A 20-channel multiplexers and one 82357B USB/GPIB interface. Note that Agilent data logger 34972A or 34980A can be used as well. The resistance measurement was done after each vibration test cycle (50 minutes) or each drop test cycle (10 drops).

Table 2. Number of Boards under reliability testing

	Cross-sectioning & SEM/EDX		Mechanical Reliability	
	Flash Au	Thick Au	Flash Au	Thick Au
Group 1: No aging	1	1	6	6
Group 2: thermal aging for 30 days at 125C	1	1	5	6
Group 3: thermal aging for 56 days at 125C	1	1	5	6



(a) Random vibration setup (b) Drop test setup

Figure 3. Setup of the random vibration and the drop test

Failure Criteria

Although solder joint reliability has been studied for over thirty years, the failure criteria are still not well defined and the relationship between the crack area of an interconnection and the change in resistance of the interconnection has not been established. Thus, different researchers use different failure criteria, for example, a resistance threshold of 450 Ω (J. Lau, et al., 2004), an increase in resistance of 10Ω or greater (M. Farooq, 2003), resistance change of 5Ω (J. Suhling, et al., 2004), a resistance threshold of 100 Ω or 20% increase in resistance if initial resistance is over 85Ω (JEDEC22-B111), and a resistance threshold of 1000 Ω (IPC-9701). In a sense, all of these criteria are subjective, because at this time no scientific research has been done on the interconnection failure criteria. Henshall et al. (2009) compared three different electrical failure criteria, 20% resistance rise, 500 Ω, and hard open (infinite resistance) and concluded that use of the IPC-9701A standard failure criterion of 20% resistance rise provides the most sensitive measure of failure among those studied.

In this project, the failure criterion is defined as an increase in resistance of 2 Ω or more from initial resistance. Our principles for establishing this criterion are 1) to detect solder joint failure as early as possible, and 2) no fault detection due to measurement error/variation. The initial daisy chain resistances in this study are between 0.75 and 2.83 Ω. We did a gauge repeatability and reproducibility (GR&R) study on the data acquisition system (Agilent data logger 34970A) and concluded that the 3 sigma of the data acquisition system was +/- 0.6 Ω. The failure analysis based on cross-section and SEM analysis confirmed that a full crack in the solder joint had occurred if the change in resistance was 2 Ω. The details of this GR&R study and the relationship between the crack size and the change of resistance will be reported in a future paper.

Results and Discussion

To compare the reliability of solder joints with different Au contents, it is important to calculate the Au content in the final solder joint. The solder joint Au content in this study was calculated according to Equation 2.

$$wt\%Au = \frac{Au \text{ weight in component } + Au \text{ weight in PCB}}{SnAgCu \text{ weight in paste } + Au \text{ weight in component } + Au \text{ weight in PCB}} \quad (2)$$

Since there is variation in Au thickness at different locations on a board, on different boards, and on different component leads, and since there is variation in solder paste volume of a package type on different pads and different boards, the nominal and range of Au content were calculated. We also found that the SAC solder wetted the tops of gold plated leads, increasing the gold that entered the solder joint. In this project, the calculation of the Au content is based on the measured solder paste volume and the measured Au thickness on PCBs and on components. The volume of solder paste on every pad of every board was measured by a solder paste inspection system. The Au coating thickness on the component and on the board was measured by an X-Ray Fluorescent (XRF) system on sample locations. The calculated Au content data in weight percentage are summarized in Table 3. It shows that there is a wide range of Au content between these five package types on two types of boards.

Table 3. Au content in weight percentage in solder joints

		QFN5	QFN6	TOPS	FPI	FPII
Flash Au board	Nominal	0.6	0.6	2.5	13.8	13.0
	Range	0.3 ~ 0.9	0.3 ~ 0.9	2.0 ~ 3.0	11.6 ~ 16.0	11.0 ~ 15.0
Thick Au board	Nominal	5.0	5.0	7.0	17.0	16.0
	Range	4.0 ~ 6.0	4.0 ~ 6.0	5.5 ~ 8.5	15.0 ~ 19.0	14.0 ~ 20.0

The number of components that failed after random vibration for 500 minutes and mechanical shock for 100 times is summarized in Table 4. The numerator in each cell refers to the number of failed daisy-chains and the denominator refers to the total number of components in the reliability test.

After examining the locations of the failed QFN5 and QFN6 components, we found that all of the failed QFN5 components occurred at location AT30, and all of the failed QFN6 components were at location U18. AT30 is located at the lower left corner of the test vehicle shown in Figure 1 and U18 is located at the upper left corner of the test vehicle. Both locations are near the mounting hole. This indicates that high strain during the board flexure in the drop and random vibration testing caused the failure of solder joints under these components. Excluding the components near the mounting holes, none of the QFN5 and QFN6 components failed in any of the test groups. Thus, we concluded that all QFN solder joints with Au content less than 5% are reliable; and thermal aging at 125°C for up to 56 days does not cause significant degradation in reliability. Note that Cu from the QFN component lead is present to diffuse into the solder joints in this case.

After examining over 25 SEM images of failed solder joints for the QFN components, we found that the failure mode on flash Au boards is different from that on thick Au board. The failure mode on flash Au boards was fracture in the Sn matrix at the bulk solder joint as shown in Figure 4. There were two failure modes of the QFN components on thick Au boards.

The first was fracture in the Sn matrix at the bulk solder joint in the as-built samples. The second failure mode is fracture through the $AuSn_4$ IMC in the thermally aged samples. After thermal aging, smaller $AuSn_4$ IMCs combined and became larger $AuSn_4$ IMCs. Figure 5 shows fracture in the bulk solder in an as-built sample and Figures 6 – 7 show fracture in the $AuSn_4$ IMC. Fractures could begin at the middle of the bulk solder, the outside of the bulk solder, as well as the IMC interface near the board or the component. We can conclude that a) if the size of $AuSn_4$ IMC is small enough, the failure mode is fracture in the Sn matrix of the bulk solder when the solder joint is under high strain; b) if the size of $AuSn_4$ IMC is large enough, the failure mode is fracture through the $AuSn_4$ IMC for solder joints under mechanical reliability testing. After further examining the location of failed solder joints on both flash Au boards and on thick Au boards, we found that it was always the solder joints closest to the mounting hole that failed. It is clear that high strain leads to the failure of these solder joints.

For the TOPS components, it appears that the reliability of solder joints on the flash Au boards is better than that of solder joints on the thick Au boards since only one failed out of 144 components on the flash Au board while 11 components failed out of 162 components on the thick Au boards. Note that seven failed components were on the same thick Au board. The SEM image in Figure 8 demonstrates that the failure mode is fracture in the $AuSn_4$ IMC. In addition to a large amount of $AuSn_4$ IMC in the bulk solder joint contributing to the failure of solder joint, voiding is another factor. We noticed that there are large voids in solder joints on all failed TOPS components on the thick Au board, although not every failed joint had large voids. It will be interesting to investigate why the voids were specific to these parts and this gold content. An X-ray image and an SEM image in Figure 9 clearly show the voids on one failed component.

Note that one significant difference between the IMC in QFN solder joints and the IMC in TOPS solder joints is that more Cu was dissolved into the solder joint from the Cu lead of the QFN component, while limited Cu was dissolved from the TOPS lead due to the Ni finish. The detailed microstructural analysis of these components will be published in a future paper. We conclude that if Ni layers exist on both the board side and the component side, which limits the Cu available to dissolve into the solder joint, an Au content less than 3% in weight is acceptable for SnAgCu solder. From the results of QFN components, we conclude that if Cu is available to dissolve in the solder joint, an Au content of less than 5% in weight is acceptable for SnAgCu lead-free solder.

For FP I and FP II components, all of the components on the thick Au boards failed (complete open or with very high resistance) immediately after assembly, while all components on the flash Au boards passed initial electrical test. About two-thirds of the components on the flash Au boards failed after the mechanical shock and random vibration testing. The cumulative failure rate of these 96 FP components on flash Au boards is shown in Figures 10 and 11. It is clear that solder joints started to fail after 1 cycle (50 minutes) of random vibration. It was observed that many FP components on the thick Au boards fell off the boards during the mechanical reliability tests. Thus, solder joints with an Au content over 10% are not acceptable.

Figure 12 shows the microstructures of a typical solder joint of a FP component. The entire solder joint consists of (Au, Ni)Sn_4 IMC with about 20 wt% of Au, 4 wt% of Ni, and 76 wt% of Sn. It is expected that the microstructures of the entire solder joint are $AuSn_4$ or (Au, Ni)Sn_4 IMC if the Au content is close to 20% in atomic fraction. Note that there is a Ni layer in the FP component, preventing diffusion of copper into the joint.

Table 4. Summary of the number of components failed after random vibration and mechanical shock tests

	Flash Au Board			Thick Au board		
	As-built	After thermal aging for 30 days	After thermal aging for 56 days	As-built	After thermal aging for 30 days	After thermal aging for 56 days
QFN5	0/54	0/45	4/45*	3/54*	3/54*	3/53*
QFN6	6/54**	5/45**	5/45**	6/54**	5/54**	6/54**
TOPS	0/54	1/45	0/45	2/54	7/54***	2/54
FP I	24/36	26/30	20/30	All daisy-chains had open solder joints after assembly		
FP II	27/36	25/30	19/30	All daisy-chains had open solder joints after assembly		

Notes: * all failed components of QFN5 are in location AT30, which is near the mounting hole
** all failed components of QFN6 are in location U18, which is near the mounting hole
*** these seven failed components of TOPS are in one board. X-ray images show that there are very large voids on many solder joints on the TOPS component.

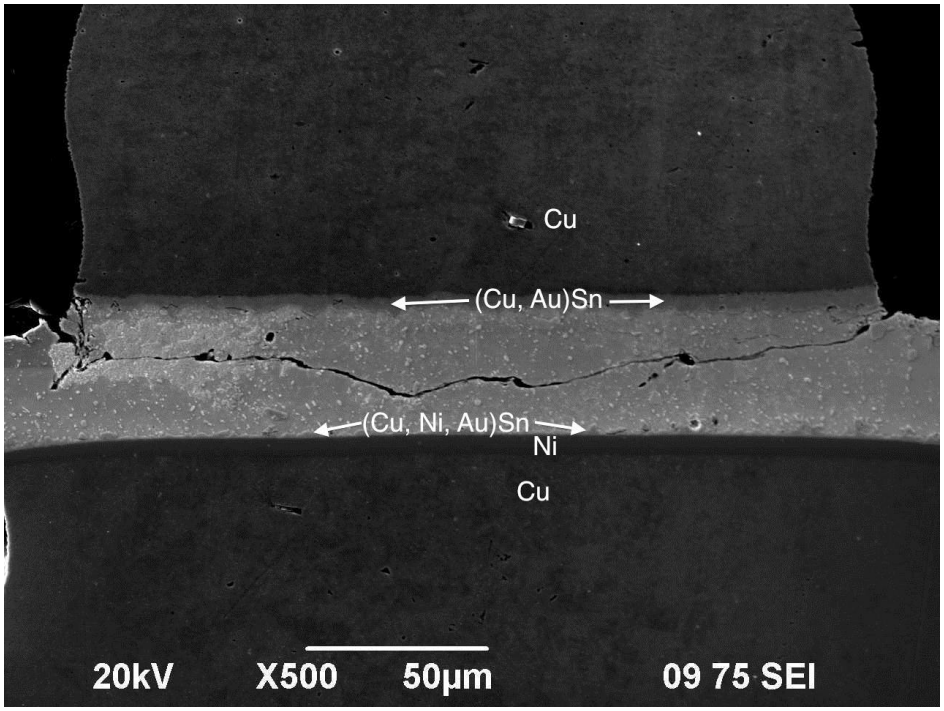


Figure 4. Fracture in bulk solder of a QFN on a flash Au board, after thermal aging for 56 days (Note, small white dots in the bulk solder are AgSn)

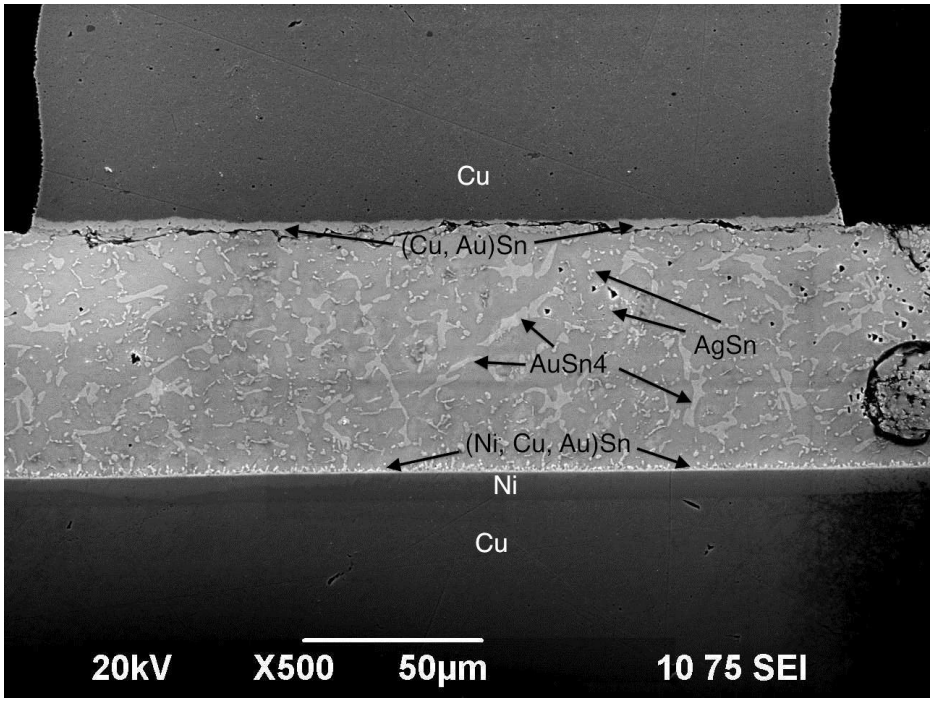


Figure 5. Fracture in bulk solder joint near component side, a QFN on a thick Au board, as built

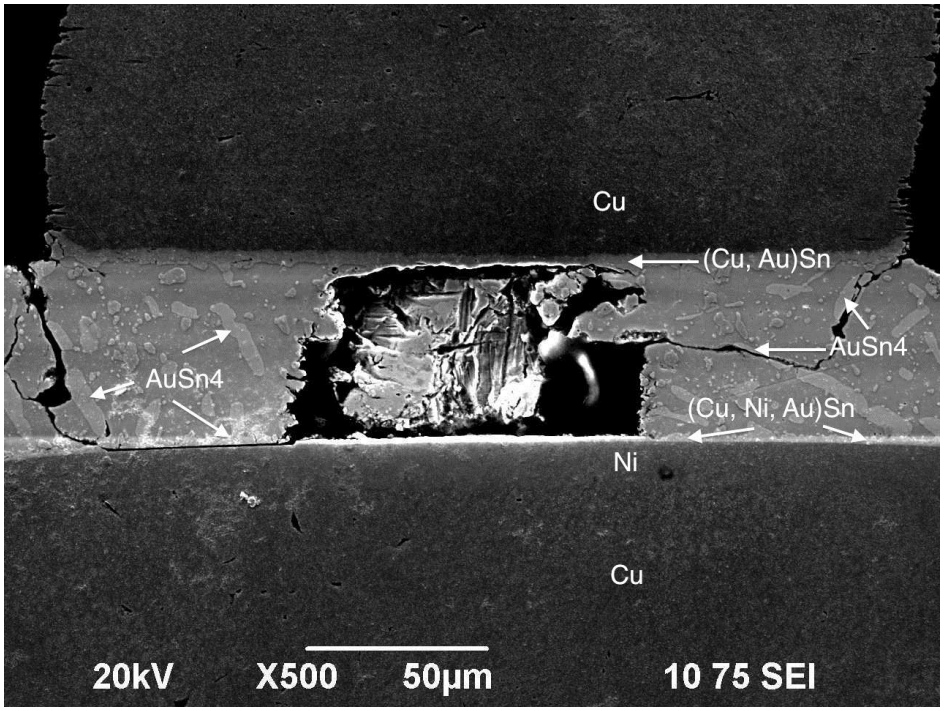


Figure 6. Fracture in $AuSn_4$ IMC in the interface near board side and crack in $AuSn_4$ IMC in the bulk solder, a QFN component on a thick Au board, after thermal aging for 56 days

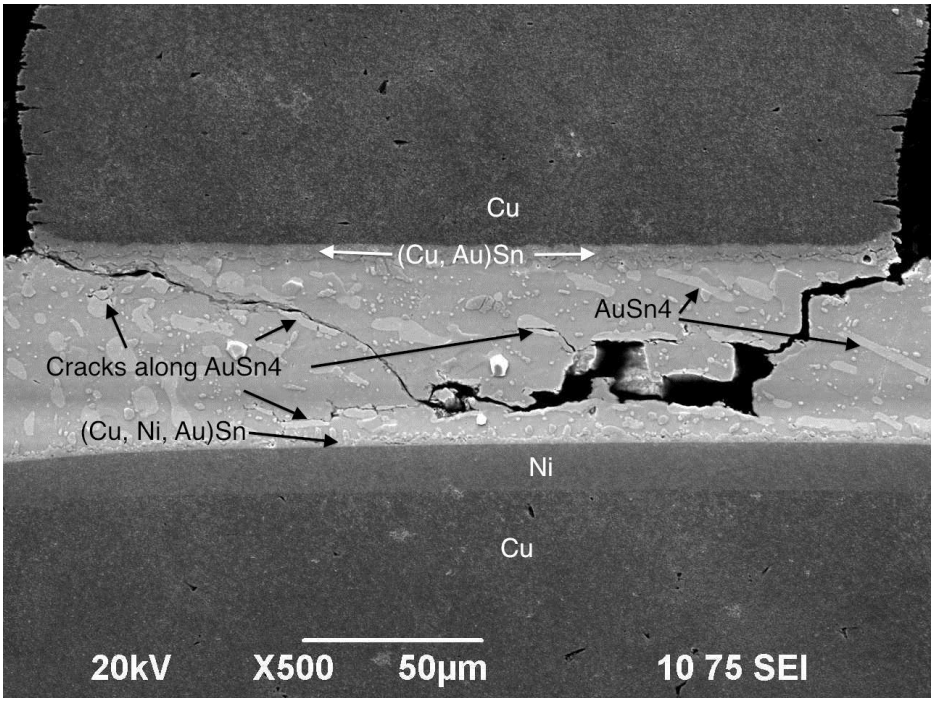


Figure 7. Fracture in $AuSn_4$ IMC in the bulk solder, a QFN component on a thick Au board, after thermal aging for 56 days

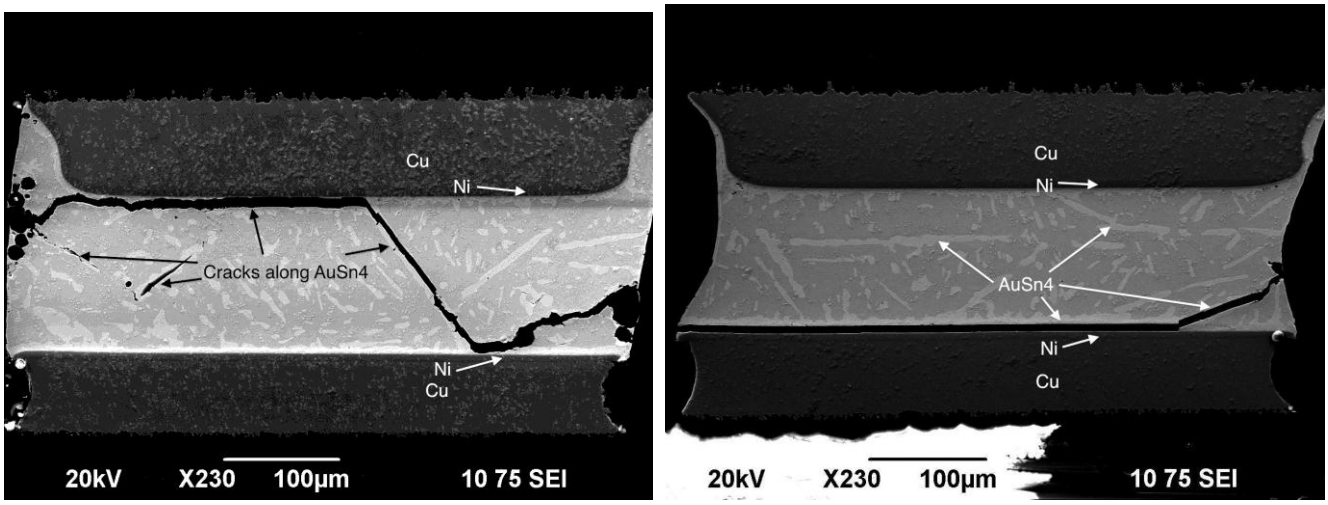


Figure 8. SEM images of solder joints of a TOPS component on a thick Au board, after thermal aging for 30 days

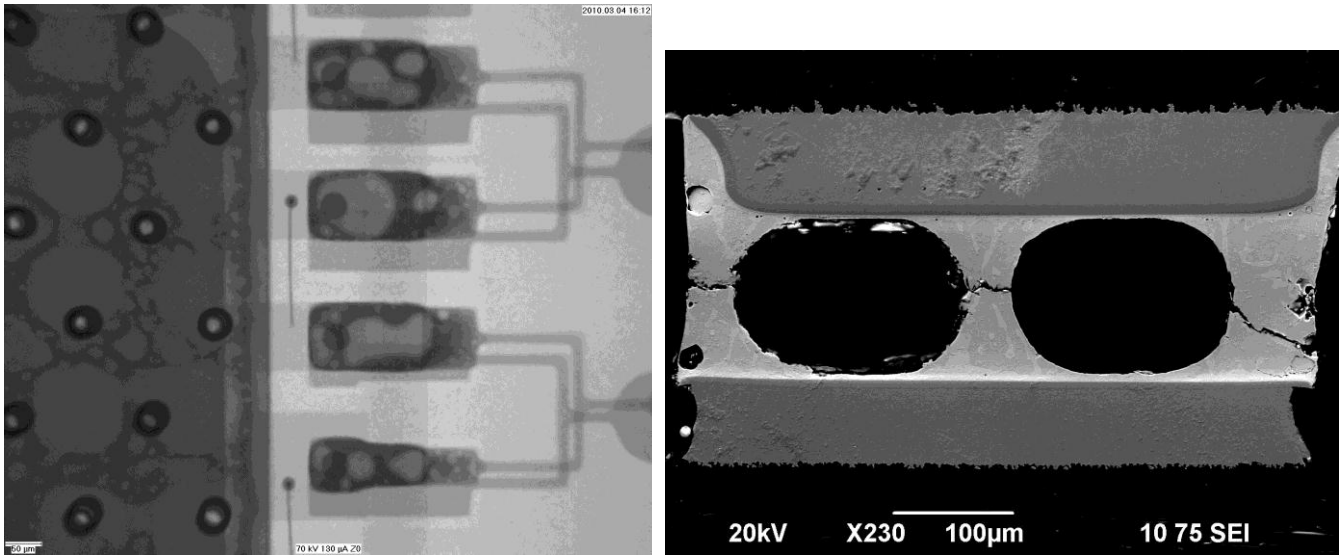


Figure 9. An X-Ray image and a SEM image showing voids in solder joints of a TOPS component on a thick Au board

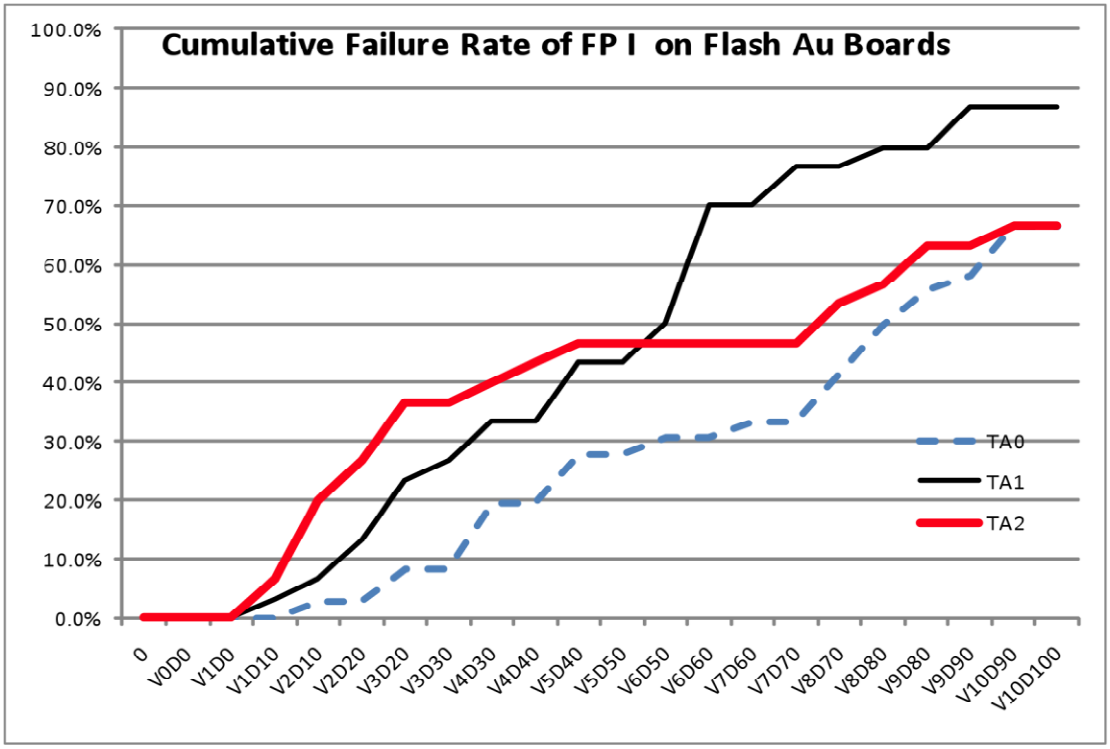


Figure 10. Cumulative failure rate of FP I components on flash Au boards. TA0 represents as-built, TA1 represents thermal aging at 125°C for 30 days, TA2 represents thermal aging at 125°C for 56 days, V1D10 in the x-axis represents 1 cycle (or 50 minutes) of random vibration and 10 drops.

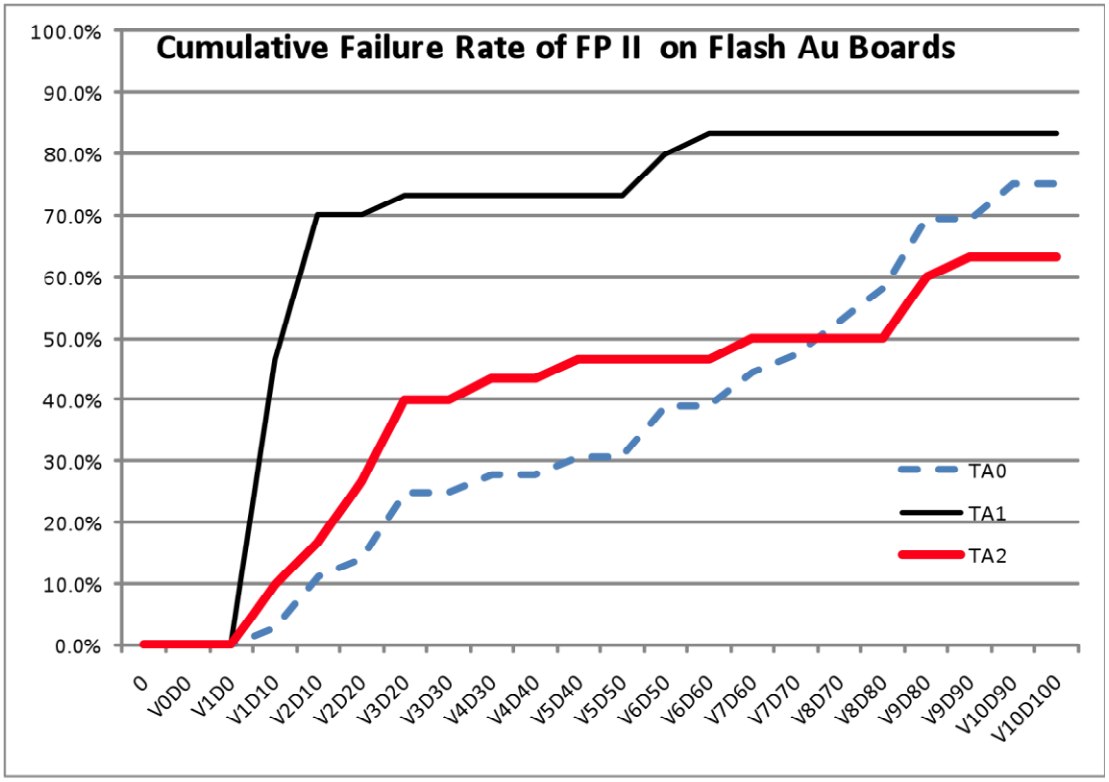


Figure 11. Cumulative failure rate of FP II components on thick Au boards. TA0 represents as-built, TA1 represents thermal aging at 125°C for 30 days, TA2 represents thermal aging at 125°C for 56 days, V1D10 in the x-axis represents 1 cycle (or 50 minutes) of random vibration and 10 drops.

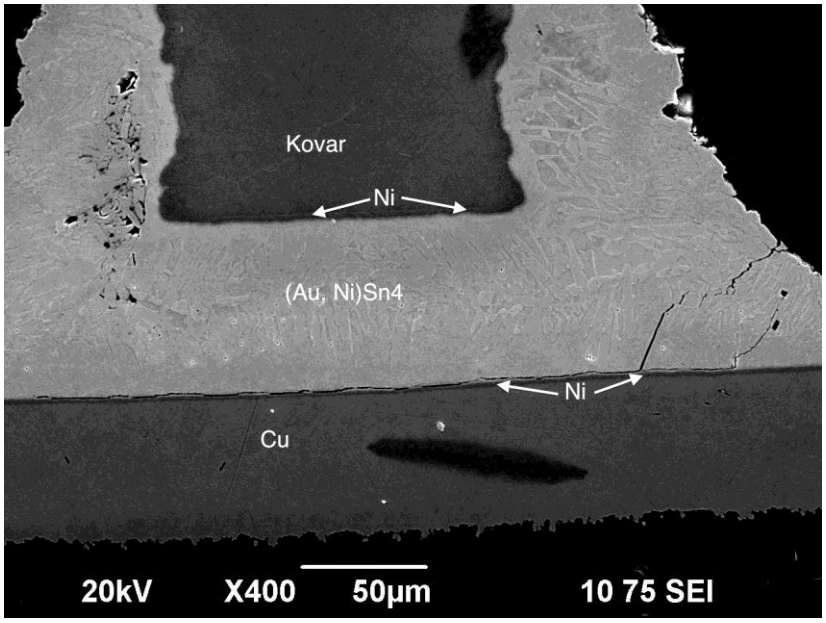


Figure 12. SEM images of solder joints of a FP component on a flash Au board, after thermal aging for 56 days

Conclusions

A comprehensive study has been conducted investigating the effect of Au content on lead-free solder joint reliability. The results show that SAC305 solder joints with over 10 wt% Au are unacceptable. If Cu is available to dissolve into the solder joint, then an Au content under 5 wt% will not significantly degrade the reliability of the solder joint. When Ni layers are present on both the board and component sides of the interface, limiting the ability of Cu to dissolve into the solder joint, an Au content under 3 wt% is acceptable. Additional findings confirmed the danger of placing parts near high stress areas and that a high level of voiding reduced reliability.

When the Au content in a solder joint is less than 3 wt%, $AuSn_4$ IMCs are small and won't play a significant role. The failure mechanism of such a solder joint is fracture within the Sn matrix when the joint is subjected to a very high stress level. If the Au content is high or large $AuSn_4$ IMCs are present in a solder joint, the failure mechanism is fractures through the $AuSn_4$ IMCs. Fractures through the $AuSn_4$ IMCs were found in the bulk solder and/or near the solder/metallization interface. Ho et al. (2002) claimed that the weak interface between (Au, Ni)Sn_4 and Ni_3Sn_4 results in brittle interfacial failure. However, our comprehensive long-term reliability study did not confirm this finding.

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