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CONFORMAL COATING EVALUATION FOR USE IN HARSH ENVIRONMENTS UTILIZING A MODIFIED SIR TEST PROTOCOL

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ABSTRACT
High reliability electronics pose a higher risk of failure when operating in harsh environments such as high temperature and high humidity. Add the possibility of ionic contaminants left on the substrate surface from the electronics manufacturing processes and you have a situation set for failure. The deadly combination of moisture (humidity), electrical potential (voltage bias), and ionic contamination (residue) is enough to create electrochemical failures such as dielectric failure and current leakage – both of which result in degradation in performance, if not complete failure, of the electronics hardware.

One common test standard used to evaluate the effects of assembly materials and manufacturing processes (i.e. residual materials) for hardware operating in hot, humid environments is the Surface Insulation Resistance (SIR) test. Although many test specifications and protocols exist, a more aggressive test protocol is required for high reliability electronics in order to determine if the materials and processes used to manufacture the electronics assembly will result in current leakage and/or dielectric breakdown between conductors. This paper will study a customized test protocol designed to environmentally stress screen conformal coatings for their ability to withstand moisture ingression and protect the conductors from moisture-related failures such as corrosion and dendritic growth formations. The analysis of data captured from continuous voltage monitoring (for dendritic growth/shorts) in addition to traditional SIR testing will provide the manufacturing engineer the necessary data to evaluate and identify the optimal material set and process parameters to manufacture high reliability electronics for operation in harsh environments.

Key words: High Reliability Electronics, Surface Insulation Resistance (SIR), Dendritic Growth, Conformal Coating, Material Qualification, Process Evaluation, Harsh Environments, Moisture Resistance

INTRODUCTION

With the state of the economy over the past few years, manufacturers of electronics materials have struggled to stay in business. The result in changing business status and business models has often led to the discontinuing/elimination of material product lines leaving design engineers with the challenge of quickly and cost-effectively qualifying new materials. Also, manufacturing and assembly has become more competitive as contract manufacturers vie for existing and new contracts thus leading process engineers the challenge to quickly and cost-effectively qualify new processes, materials, and manufacturing equipment.

Thus, a cost-efficient and effective test protocol is needed to assess these changes in today's dynamic electronic industry. This test protocol can be used to qualify new and existing materials, compare similar materials or processes, and/or establish performance characteristics in the intended end-use environment [1].

SIR TESTING

Surface Insulation Resistance (SIR) testing is a commonly used test method to qualify materials and processes for the electronics industry [2]. SIR testing measures the change in current over time between two electrical conductors and is indicative of inadequate electrical isolation due to a breakdown in the insulating materials, e.g. solder mask, conformal coat, etc. Traditional SIR is performed by applying a voltage to conductors on a printed wiring board (PWB) and measuring the returning current. Simple calculation by Ohm's Law results in the insulation resistance (IR) between non-common conductors. SIR testing is typically performed under application of heat and/or humidity. However for high reliability (high-rel) electronics, a more aggressive test protocol is needed to mitigate failure when operating in harsh environments.

Evaluation Criteria

In the hi-rel sector of the electronics industry, circuit card assemblies (CCAs) are extremely sensitive to a number of variables including assembly materials, manufacturing processes, design parameters, and operating environment. Therefore, test protocols such as SIR as used to qualify, compare, and/or establish characteristics of these variables.

- Assembly Materials
  - PWB Fabrication Materials
  - Conformal Coating Materials
  - Solder Paste
  - Solder Flux
- Manufacturing Processes
  - Cleaning Process

- Design Parameters
  - Voltage Bias
  - Component Lead Pitch
  - Component Lead Geometry
  - PWB Trace Width/Spacing
- Operating Environment
  - Humidity
  - Temperature
  - Vibration/Shock
  - Ingression (Salt/Sand)

The deadly combination of moisture (operating environment), electrical potential (design parameters), and ionic contamination (assembly materials and manufacturing processes) is enough to create electrochemical failures such as dielectric failure and current leakage – both of which result in degradation in performance, if not complete failure, of the electronics hardware.

The failure mechanism driving dielectric failure and current leakage is attributed to metal migration, i.e. dendritic growth between two non-common conductors. Dendritic growth occurs when the combination of ionic contaminants, moisture, and an electrical potential are present and results in the reverse plating of metal conductors [2]. These dendrites, i.e. metal conductors, grow from a positively charged conductor to a negatively charged conductor resulting in a low-resistance metal bridge and thus an IR failure. Hence the reason SIR testing is typically used to evaluate materials (conformal coating) and processes (cleanliness) designed to protect the electronic assemblies.

Several industry standards exist to perform SIR testing. Test standards and test vehicles have been developed by IPC, Bellcore, and JIS. Each protocol uses a variation of test environment, test duration, measurement frequency, voltage bias, and test vehicle design. The test vehicles contain patterns, typically interdigitated combs, and/or components designed to provide insulation resistance monitoring at various intervals. A summary of these is provided below in Table 1 [3].

CUSTOMIZED SIR TEST PROTOCOL

While these test protocols and test coupons exist, a more aggressive test protocol and customized test vehicle are required for high-rel electronics in order to determine if the materials and processes used to manufacture the electronics assembly will result in current leakage and/or dielectric breakdown between conductors.

A customized test protocol is recommended that is designed to environmentally stress screen manufacturing processes and assembly materials, such as conformal coatings, for their ability to withstand moisture ingression and protect the conductors from moisture-related failures such as corrosion and dendritic growth formations, due to remaining manufacturing process residues but also to specifically assess the ability of the applied conformal coating to penetrate under low-profile and area-array devices in addition to edge-and-point coverage of conventional leaded devices.

A materials qualification test protocol is available to satisfy these requirements that utilizes a modification to standard SIR test procedures and offers an accelerated method to qualify assembly materials and manufacturing processes. With faster data sampling rates and a more aggressive test environment, the materials qualification test protocol is designed to provide a cost-efficient, quick-turn evaluation of both assembly materials and manufacturing processes through industry standard SIR testing and customized supplementary voltage monitor testing. A customized test vehicle is designed, e.g. line width/spacing and component set, and manufactured, e.g. assembly materials and cleaning processes, as closely as possible to those employed by the current manufacturer. Standard test patterns, such as the interdigitated comb patterns, may also be integrated into the customized test vehicle.

Cyclic humidity and temperature test conditions, such as those specified in IPC-TM-650 Method 2.6.3.4 [4] and MIL-STD-202 Method 106 [5], in addition to application of a bias voltage, are utilized to intensify the effect of humidity and temperature cycling to determine if the materials (conformal coating) and processes used to manufacture the

Table 1. Standard Industry SIR Test Protocols.

STANDARD	IEC 61189-5 (In draft)	ISO 9455-17 (Latest)	J-STD-001C	IPC-TM-650 2.6.3	IPC-TM-650 2.6.3.3	Bellcore
Temperature/ Humidity	40°C/93% RH	85°C/85% RH	85°C/85% RH	Class 1 - 35/90°C at 98% RH for 4 days static Class 2 - 50/90°C at 98% RH for 7 days static Class 3 - 25/65°C at 90/98% RH for 7 days cycling	85°C/85% RH	35°C/85% RH
Test Duration	72 Hours	168 Hours	168 Hours	168 Hours	168 Hours	120 Hours
Measurement Frequency	Measured at 20min intervals	Measured twice a day	Measured at 24hrs, 94hrs and 168hrs	Measured at 24hr intervals	Measured at 24hrs, 94hrs and 168hrs	Measured at 25hrs and 120hrs
Test voltage Bias	5V +5V	50V +50V	100V –50V	100V –50V	100V –50V	100V –50V
Test Coupon	Under review	IPC-B-24	IPC-B-36	IPC-B-25A	IPC-B-24	IPC-B-25A

CCA will result in current leakage and/or dielectric breakdown between conductors. Due to the nature of electrochemical failure mechanisms such as metal migration/dendritic growth to form and then "blow", methods are used to capture and preserve these formations. One method commonly used is to wire the test vehicles with current-limiting resistors to help preserve dendrite formation. Another method is to increase the data sampling frequency as implemented in the customized SIR test protocol.

Increased data sampling rates better equip engineers with the necessary data to make design, materials, and process parameter decisions. Per the customized test protocol, voltage monitoring of the current-limiting resistors per the applied voltage bias is captured every 60 seconds throughout the duration of the test – a 20X improvement over standard SIR tests data capture rates – thus providing greater opportunities to capture electrochemical degradation, i.e. dendritic growth. In addition to voltage monitoring, insulation resistance measurements are taken at the end of each temperature/humidity cycle (i.e. every 24hrs) per SIR test requirements. Analysis of the IR data captured during daily SIR testing and of the continuous voltage monitoring (every 60 seconds) will provide a comprehensive data set in order to effectively identify and evaluate the optimal materials and process parameters to manufacture high reliability electronics for operation in harsh environments.

CASE STUDY: CUSTOMIZED TEST PROTOCOL

A customized test protocol was created in order to evaluate and compare the edge-and-point coverage capability of three conformal coatings for qualification on a high-rel CCA used in a high temperature, high humidity (condensing moisture) environment. Due to scheduling requirements, an existing test coupon (see Figure 1) was used as the test vehicle for the study with focus on the specific types of component packages currently in use on the CCA. IPC's Standard B-52 Cleanliness & Residue Evaluation Test (CRET) PWB was used for this test protocol [6].

Test Vehicle Design

True dummy components (isolated conductors with no internal die, wire bonds, or interconnections) were procured, and the CCA was manufactured using as closely as possible the manufacturing process employed by the current manufacturer, i.e. solder paste, cleaning process, conformal coating application. The components utilized in the customized test protocol were as follows:

- **TQFP** 80-lead device, 0.5mm pitch, gull-wing lead configuration, 12mm body
- **QFP** 160-lead device, 0.65mm pitch, gull-wing lead configuration, 28mm body
- **SOIC** 16-lead device, 0.8mm pitch, gull-wing lead configuration, 3.8mm body

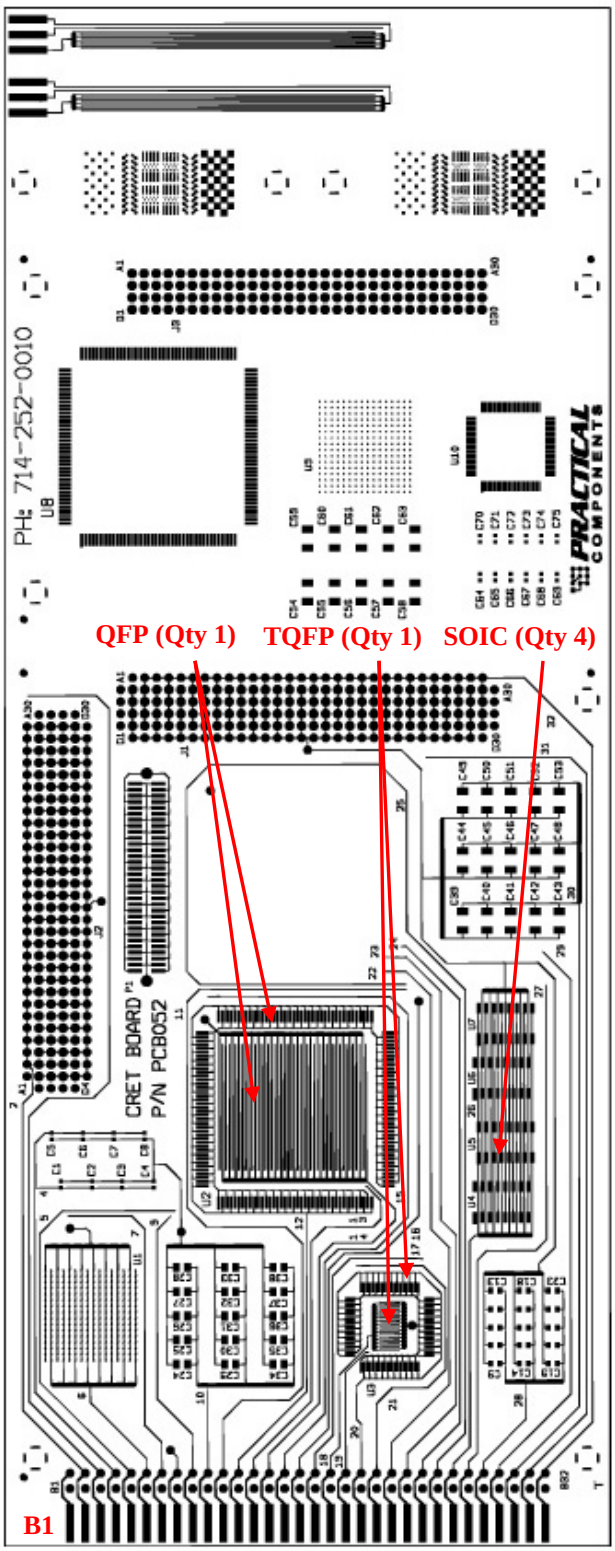

Figure 1. IPC's Standard B-52 CRET PCB (Top Side).

The test patterns monitored in the customized test protocol included a conglomeration of interdigitated combs and adjacent component leads. The interdigitated combs were located underneath the component bodies and would result in decreased insulation resistance should residues become entrapped. Monitoring of adjacent component leads enable

evaluation of coverage capability of fine-pitch, sharp-edged, leaded devices. The test patterns utilized on the IPC B-52 PCB in the customized test protocol are shown in Table 2.

Table 2. Test patterns for customized test protocol.

Device	Comb Pattern		Component Lead Pattern
TQFP80	127um LW	178um LS	0.50mm pitch
QFP160	305um LW	250um LS	0.65mm pitch
SOIC16	205um LW	215um LS	N/A

Customized Test Parameters

A 64-conductor cable assembly was soldered directly to the test pads along the bottom edge of the test vehicle. The cable assembly was used to interconnect the test patterns on the test vehicle to the polarized voltage bias and to subsequently be disconnected and to interconnect to the SIR test equipment for IR testing. The test vehicles were locally cleaned with IPA after the wires from each lead were soldered to the assemblies, and the leads were thoroughly covered with sealant to eliminate the cable assembly as a potential cause of failure.

Current-limiting resistors of 1MΩ resistance value were wired in series on the return path to the voltage supply to prevent excessive current flow in the event of a short. The test vehicles were placed in the chamber in a horizontal configuration (see Figure 2) such that condensation may accumulate on the assemblies' surfaces (similar to that of the actual operating environment of the CCA).

Figure 2. Temp/Humidity Test chamber configuration.

Based on the actual operating environment of the CCA, the traditional temperature and humidity testing was replaced by a more aggressive profile based on a modification of the Moisture Resistance test profile per MIL-STD-202G Method 106G [4] (see Figure 3). The temperature was cycled between 25°C and 65°C while maintaining 95% RH at soak and a minimum of 90% while in transition. The transition time between soaks was reduced in order to induce a condensing environment to simulate that of the actual operating environment of the CCA.

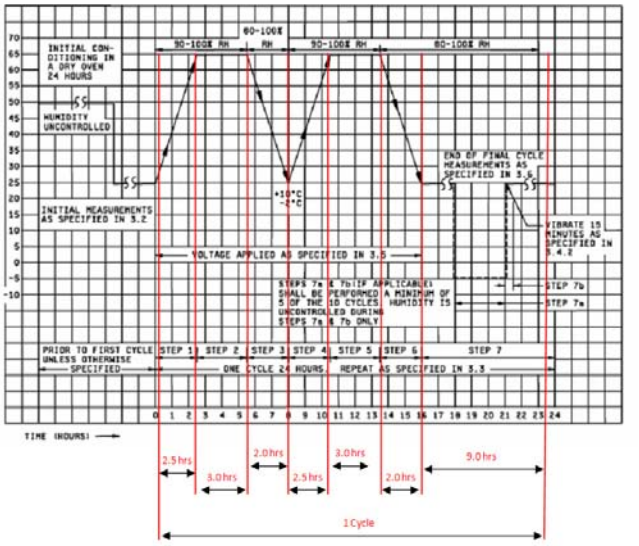

Figure 3. Modified temperature/humidity profile.

Initially, the test vehicles were conditioned for 24 hours at 50°C with no added humidity. Directly following the conditioning, the test vehicles were exposed to 10-cycles of the modified temperature/humidity profile as shown in Figure 3 with an applied 50V voltage bias. Based on the comb pattern spacing, a maximum voltage gradient of 280 V/mm is achieved (TQFP80 comb spacing) with a minimum of 77V/mm (QFP160 component lead pitch) on the test vehicle.

During testing, a data acquisition system monitored the voltage drop across the current-limiting resistors to capture drops in resistance indicative of dendritic growth between combs or leads. The data acquisition monitored 5 channels (see Table 2) per test vehicle with a data capture frequency of 60 seconds. The data captured was plotted to correlate resistance change versus time versus temperature and provided real-time monitoring of moisture-related failures.

Prior to the initial cycle and at the end of every cycle, the voltage bias was disconnected and a SIR test was performed at 100VDC with a 60 second soak. The minimum allowable insulation resistance between conductors is 100MΩ (or $1x10^8$ Ohms). The test vehicles were not removed from the chamber throughout the 10-cycles. Upon completion of testing, a final SIR test was performed 48 hours after the final cycle with the test vehicles maintained at 25°C with no added humidity.

Test Results

The SIR test results were correlated to the voltage monitoring test data and plotted versus time and temperature. It is common knowledge that SIR data is dependent on the geometry of the test pattern and therefore data between test patterns differing in geometry may not be directly compared [6]. Therefore, like patterns on test vehicles with different materials (e.g. conformal coating material) and/or processes (e.g. coating application process) should be evaluated whereas data between dissimilar

patterns cannot be directly compared. The results of the SIR test data is shown in Table 3.

Table 3. SIR test data for conformal coating evaluation.

Serial Number 001 - Coating A					
Cycle	QFP (leads)	QFP (comb)	TQFP (comb)	TQFP (leads)	SOIC (comb)
Initial	1.60E+09	3.21E+09	3.87E+09	3.62E+09	2.72E+09
50°C Cond	4.52E+09	8.42E+09	6.89E+09	5.86E+09	3.34E+09
1 cycle	1.61E+09	1.27E+09	1.88E+09	1.72E+09	6.65E+08
2 cycle	9.16E+08	7.38E+08	6.36E+08	2.38E+08	4.14E+08
3 cycle	8.98E+08	8.01E+08	8.44E+08	1.59E+08	4.10E+08
4 cycle	6.95E+08	6.41E+08	8.66E+08	1.32E+09	4.02E+08
5 cycle	4.04E+08	3.75E+08	5.48E+08	8.37E+08	1.99E+08
6 cycle†	8.69E+08	8.05E+08	9.86E+07	4.97E+08	4.80E+08
7 cycle‡	2.48E+08	3.07E+08	8.95E+07	1.44E+09	2.38E+08
8 cycle‡	3.43E+08	3.97E+08	7.18E+07	1.87E+09	3.10E+08
9 cycle‡	3.74E+08	3.51E+08	5.77E+07	1.18E+09	2.61E+08
10 cycle‡	2.58E+08	3.24E+08	1.02E+08	1.02E+08	2.81E+08
48hr Post	3.86E+09	3.23E+09	2.31E+09	3.43E+09	3.43E+09
Serial Number 002 - Coating B					
Cycle	QFP (leads)	QFP (comb)	TQFP (comb)	TQFP (leads)	SOIC (comb)
Initial	1.16E+09	1.23E+09	2.47E+09	1.32E+09	2.50E+09
50°C Cond	1.65E+09	8.12E+08	1.22E+09	1.23E+09	3.67E+09
1 cycle	2.45E+08	8.23E+06	3.42E+07	6.42E+07	6.54E+08
2 cycle	2.24E+08	5.96E+06	9.63E+07	3.14E+07	4.73E+08
3 cycle	1.76E+08	2.58E+06	1.71E+08	1.35E+07	5.25E+08
4 cycle	1.38E+08	6.17E+06	2.00E+08	8.06E+06	5.72E+08
5 cycle	2.11E+08	6.54E+06	2.62E+07	1.22E+07	4.46E+08
6 cycle†	1.56E+08	4.28E+06	1.29E+06	6.66E+06	8.08E+08
7 cycle‡	1.25E+08	3.32E+06	D.F.	5.69E+06	3.17E+08
8 cycle‡	1.69E+07	4.83E+06	2.38E+06	3.38E+06	3.18E+08
9 cycle‡	2.87E+07	4.37E+06	D.F.	2.06E+06	2.16E+08
10 cycle‡	4.74E+07	4.12E+06	D.F.	3.02E+06	2.04E+08
48hr Post	8.16E+08	1.15E+08	7.68E+06	8.83E+07	3.75E+09
Serial Number 003 - Coating C					
Cycle	QFP (leads)	QFP (comb)	TQFP (comb)	TQFP (leads)	SOIC (comb)
Initial	1.38E+09	1.44E+09	3.04E+09	1.52E+09	2.91E+09
50°C Cond	7.47E+08	6.21E+08	4.11E+09	1.14E+09	2.83E+08
1 cycle	4.06E+08	2.94E+07	1.88E+07	1.41E+08	3.75E+08
2 cycle	5.94E+07	2.62E+07	4.91E+06	1.03E+08	1.49E+08
3 cycle	1.55E+08	3.00E+07	3.49E+06	8.76E+07	6.85E+06
4 cycle	3.59E+07	D.F.	2.94E+06	7.28E+07	2.57E+06
5 cycle	2.26E+08	1.05E+07	5.77E+06	D.F.	2.33E+06
6 cycle†	4.36E+08	2.91E+06	1.39E+06	8.68E+07	2.47E+06
7 cycle‡	D.F.	O.C.	3.48E+06	4.71E+07	1.21E+08
8 cycle‡	2.29E+06	D.F.	D.F.	2.90E+07	1.30E+08
9 cycle‡	O.C.	1.28E+06	D.F.	2.01E+07	2.00E+08
10 cycle‡	D.F.	O.C.	D.F.	1.62E+07	3.19E+07
48hr Post	4.26E+07	1.69E+07	5.24E+07	4.13E+08	3.50E+09

Failed SIR: insulation resistance < 100Mohm (1E+08)

D.F.: Dielectric Failure [attributed to excessive capacitive current (spikes) and discharge during hipot test]

O.C.: Over Current [attributed to detected shift in level of current flow during hipot test, i.e. leakage]

† Rotated boards from a horizontal orientation to a vertical orientation aligned in center of chamber for this cycle only.

‡ Additional moisture was added to the board at 25°C to ensure that moisture globlets were present on the test substrates' surfaces.

The results of the voltage monitoring test are shown in the figures below for each test vehicle. Plots are generated for each cycle and provide an analysis of insulation resistance per test pattern in regards to the current temperature/humidity state within the environmental chamber.

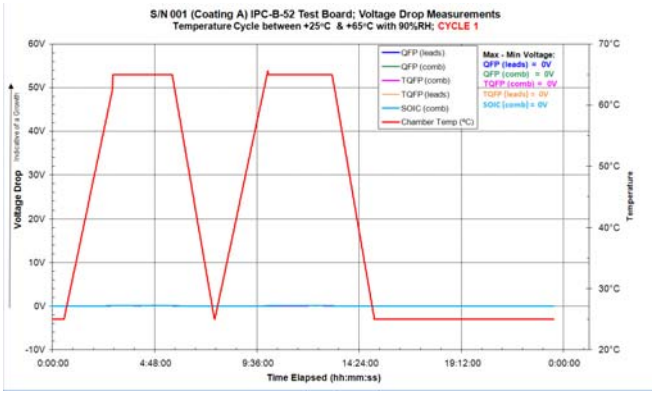

Figure 4. Serial Number 001 voltage monitoring results after completing Cycle 1.

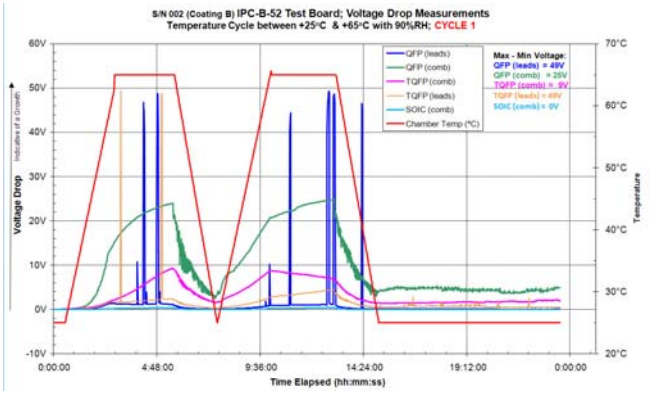

Figure 5. Serial Number 002 voltage monitoring results after completing Cycle 1.

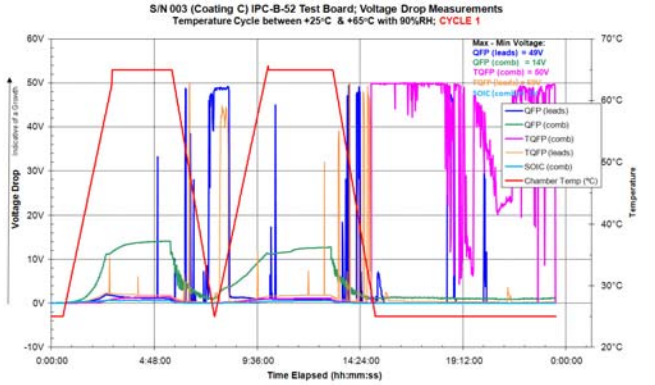

Figure 6. Serial Number 003 voltage monitoring results after completing Cycle 1.

Note: For the length of this paper, data for Cycle 2 through Cycle 9 have been omitted. Please contact the author to request this information.

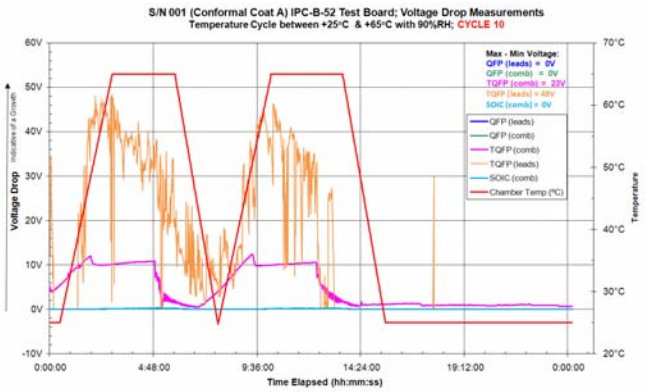

Figure 7. Serial Number 001 voltage monitoring results after completing Cycle 10.

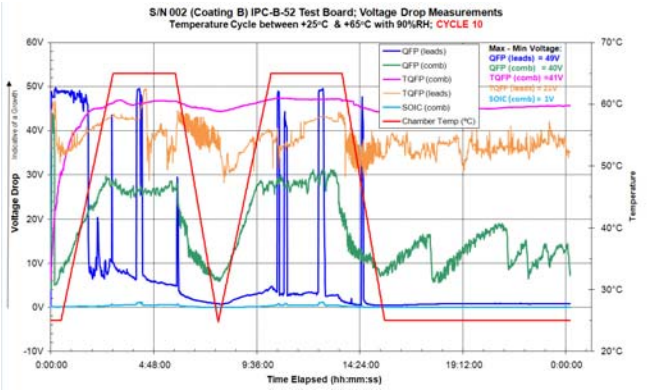

Figure 8. Serial Number 002 voltage monitoring results after completing Cycle 10.

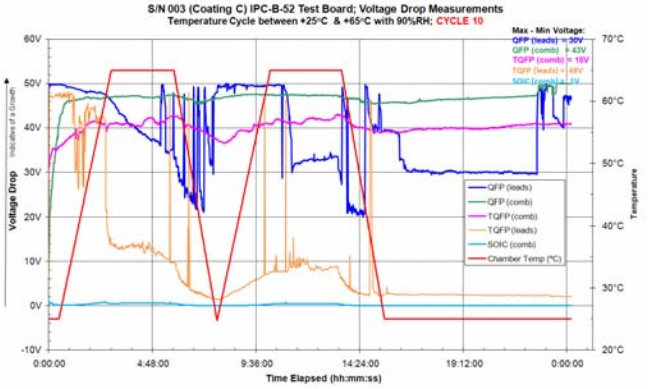

Figure 9. Serial Number 003 voltage monitoring results after completing Cycle 10.

CONCLUSION

The Initial SIR data and the SIR data captured after 50°C conditioning with no added humidity showed no signs of degradation in insulation resistance, as expected.

Voltage monitoring data collected throughout the first cycle indicated metal migration activity, particularly in the 65°C soak period, and was confirmed with the SIR data captured.

The following summary is for the three test vehicles after completing 1st cycle of temperature/humidity testing.

- S/N 001 (Conformal Coat A)
  - SIR Testing – all passed
  - Voltage Monitoring – all passed showing no signs of moisture-related failures for the duration of the cycle
- S/N 002 (Conformal Coat B)
  - SIR Testing
    - QFP (leads) and SOIC (comb) passed
    - QFP (comb), TQFP (comb & leads) failed
  - Voltage Monitoring
    - SOIC (comb) passed showing no signs of moisture-related failures for the duration of the cycle
    - QFP (leads) failed showing spikes in voltage with several hard shorts however ultimately passing while at ambient which confirms the passing SIR test
    - QFP (comb), TQFP (comb & leads) failed showing metal migration activity, particularly in the QFP comb pattern, which continued through the ambient step thus confirming the failed SIR test results
- S/N 003 (Conformal Coat C)
  - SIR Testing
    - QFP (leads), TQFP (leads), and SOIC (comb) passed
    - QFP (comb) and TQFP (comb) failed
  - Voltage Monitoring
    - SOIC (comb) passed showing no signs of moisture-related failures (>2V activity required to constitute a failure) for the duration of the cycle
    - QFP (leads) & TQFP (leads) failed showing spikes in voltage with several hard shorts however ultimately passing while at ambient which confirms the passing SIR test
    - QFP (comb) & TQFP (comb) failed showing metal migration activity, particularly in the TQFP comb pattern, which continued through the ambient step thus confirming the failed SIR test results

Voltage monitoring data continued to be collected throughout remaining cycles. For the length of this paper, only the first and final cycle will be reported.

The following summary is for the three test vehicles after completing the 10th cycle of temperature/humidity testing.

- S/N 001 (Conformal Coat A)
  - SIR Testing
    - all passed
  - Voltage Monitoring
    - QFP (leads & comb) and SOIC (comb) passed showing no signs of moisture-related failures for the duration of the cycle
    - TQFP (leads) failed showing spikes in voltage with several hard shorts however regained insulating properties while at ambient which confirms the passing SIR test
    - TQFP (comb) failed cyclically with high-resistance shorts however regained insulating properties while at ambient which confirms the passing SIR test
- S/N 002 (Conformal Coat B)
  - SIR Testing
    - SOIC (comb) passed
    - QFP (leads & comb) and TQFP (comb & leads) failed with a dielectric failure (DF) indicating excessive capacitative current (spikes) and discharge during SIR testing
  - Voltage Monitoring
    - SOIC (comb) passed showing no signs of moisture-related failures for the duration of the cycle
    - QFP (leads) failed showing spikes in voltage with several hard shorts however marginally failed while at ambient which confirms the failing SIR test
    - TQFP (comb & leads) and QFP (comb) failed continuously showing metal migration activity, particularly in the TQFP comb pattern, which continued through the ambient step thus confirming the failed SIR test results
- S/N 003 (Conformal Coat C)
  - SIR Testing
    - all failed with both DF failures (see above) and over current (OC) failure indicating dendritic growth between the QFP comb pattern.
  - Voltage Monitoring
    - SOIC (comb) failed showing diminutive signs of moisture-related failures for the duration of the cycle
    - QFP (comb & leads) and TQFP (comb & leads) failed showing spikes as well as continuous failure in voltage which confirms the failing SIR test results of DF and OC.

In summary, the analysis of data captured from both continuous voltage monitoring and traditional SIR testing provides the design engineer with the comprehensive data to evaluate and identify the optimal material set and process parameters to manufacture high reliability electronics for operation in harsh environments.

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