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THE POTENTIAL OF STENCIL TECHNOLOGY – CHOOSING THE RIGHT STENCIL OPTIONS TO MAXIMIZE YIELD AND EARNINGS

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ABSTRACT:
Miniaturization, a growing need for more functionality and low production cost are the highest aims for electronic products, especially for mobile devices. The combination of these claims lead to complex substrates and production processes. Highly integrated components help to concentrate functionality on a very small footprint, bringing fine pitches and small connection pads / pins to the substrate (like QFN, MLF, µBGA). Fine pitch and small pads increase the printing process standards. This can be countered with a thinner stencil thickness. But almost all electronic products also include components with a need for a high amount of solder volume (e.g. connectors, mechanical strained components, power components). This component mix demands a detailed set-up of the printing tool to be able to maintain a high yield at low production costs.

This document introduces stencil technologies, which address these claims and help to increase the first pass yield of your production line:

Layout optimization directly addresses production process issues like tombstones, coplanarity, bridging, solder beading and voiding. Also processes like Through Hole Reflow (THR / PiP) or leadless components (OFN / MLF) should be designed regarding a detailed solder volume calculation.

Step Stencil Technology combines different stencil thicknesses into one stencil, allowing the correct solder volume for each component. Also this technology can be used to implement cavities into the substrate side of the stencil to overcome substrate issues like too high solder resist, too high via filling or plugging, labels or overtop clamping.

3-D-Stencils are capable to print simultaneously on different height levels of a substrate and extend the usability of stencils into new areas.

PLASMA Stencils are coated with a high tech material to enhance paste release, reduce the need for cleaning and minimize the effect of line down times to volume transfer. By choosing the right combination out of the possible options you will be able to speed up your production, enhance your quality and yield.

Key words: miniaturization, 3-D stencil, layout optimization, step stencil, plasma coating

INTRODUCTION:
The key to the global electronic market is cost effective production process. Quality and yield are directly linked to the solder printing process – just a sufficient and constant paste depot is able to grant a good and stable soldering process.

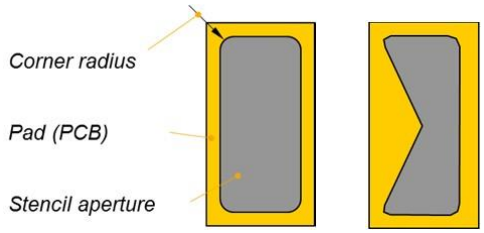

Figure 1. Typical layout optimization and a sample of a concave layout to prevent tombstones and mid chip solder beading.

But how are these goals achieved? Normally stencil openings are reduced relatively to the pad dimensions to establish a good sealing between stencil aperture and pad, aperture corners are rounded to prevent solder particles from sticking in the corners, specialized shapes help to overcome issues with tombstones or mid chip solder beading and past volume calculations are performed to provide the correct amount of solder for sophisticated components or applications like bottom terminated components (BTC) or pin in paste processes.

This may sound quite easy but the devil is in the details: Determining perfectly right parameters for the measures above requires often detailed knowledge of the complete production process. This information is not directly available for the stencil manufacturer. Experience and volume calculations can help to enhance the outcome of stencil layout optimization but cannot compensate the positive effect of a good and direct feedback from production results to the stencil manufacturer.

This is the main reason why we installed our own application center. With our own printing and measuring equipment we are able to judge our own products, enhance existing products and develop new printing tools.

TEST EQUIPMENT:
3-D-paste inspection systems allow a very detailed and reliable analysis of the actual printing performance. These systems are ideal tools to optimize printing processes and develop new instruments to conquer typical issues for

printing processes. In our application center we use Koh Young solder paste inspection (SPI) systems. For these tests a desktop system (KY 3020T) and inline version (KY 8030-3) were used to measure the transferred paste volume, collect and analyze the data.

Our print tests are performed on an Ekra X5 professional or an Ersa S1. Some of the production substrates are printed with Dek Horizon printers.

The solder paste varies in all tests; typically it is given by the product and customer specifications.

Data is produced by print test in our application center or in a production environment.

In our application center we try to eliminate as much as possible influences on the print process to be able to see just the influence of the stencil on the process. In detail this implies:

Substrate: stable structure, wrapped <1% of diagonal, surface flatness «25 µm, fully supported and no deflection under squeegee force.

Environment: constant temperature and constant humidity.

Printing equipment: perfectly maintained and calibrated. This controlled and ideal environment is used to judge just the effect of the stencil. The final approval of a new stencil option is always performed in production environment. Here typical a lot of the above mentioned influences are not ideal. But new stencil options allow resolving issues, driven by the substrate layout or quality.

MINIATURIZATION & COMPONENT MIX:

Very often the room on a substrate is very limited, therefore smaller component sizes and pitches are used. This alone is not troubling the print process. Smaller apertures and pitches are easily overcome with smaller stencil thicknesses. A clear shift from (150 … 180) µm to (90 … 120) µm is noticeable in the last years. Also surface mount technology (SMT) products with a stencil thickness of 60 µm are becoming more common.

Figure 2. Automotive PCB with high component mix.

This trend is working fine with all fine and delicate structures, but leads to trouble with bigger components such as power devices, connectors and components with coplanarity issues. These devices need more solder volume as a thin stencil can supply and often the use of preforms is to not possible or too expensive.

This component mix is the most demanding challenge for the modern stencil print process and often the biggest obstacle on the way to establish a high yield at low production costs.

By a clearly structured and detailed stencil layout in combination with a good choice of stencil options the challenges of the component mix can be addressed.

STENCIL LAYOUT:

The standard tools of stencil layout like area ratio, solder sphere rule, reduction, rounded corners and sectioning of big apertures are good to enhance the printing process [1]. But for detailed work on production yield and costs a deeper look is needed: A wide range of layout changes and stencil options is available to optimize the production process. Layout optimization is aiming for three main targets:

1. Offering the correct solder paste volume for a good solder joint.
2. Defining an opening (aperture) shape easy to print and clean.
3. Setting a solder paste depot easy to populate with components and good to reflow.

As soon as the demands are clearly stated the designer can adapt the aperture volume to the needs of the solder joint, implement specialized shapes (if needed), adjust the stencil thickness to meet the correct area ratio, check the solder sphere rule and choose the proper surface finish for the stencil.

The stencil manufacturer will supports the optimization process with suggestions and, if needed, with the implementation of the changes into the data.

VOLUME CALCULATION:

Some components are very sensitive for a certain solder volume. Especially BTC components need the correct amount of solder for their thermal and IO connections. Otherwise issues like bridging or skewing may occur.

Volume calculations are also needed to set-up the right solder volume for pin in paste applications, to conquer coplanarity issues or differences of the wet able area for ball grid arrays (BGA).

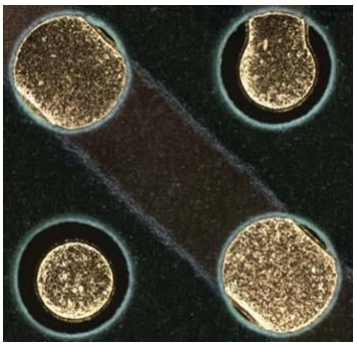

Figure 3. Pad area variation at a µBGA pitch 0,5 mm. Indirectly the solder volume calculation for thermal pads can also reduce voiding by minimizing the offered amount of solder paste.

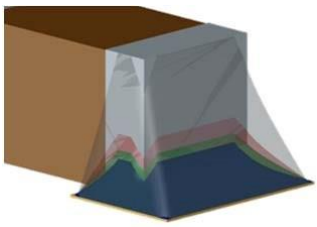

Figure 4. Solder volume calculations:
blue = minimum, green = actual status, red = average volume, grey = maximum.

For the calculation of the required solder paste volume the geometrical dimensions of the substrate pads and the wet able areas of the component are taken in account. Together with requirements of the IPC-A-610 the shape of the solder joint is defined and the solder volume calculated.

STEPPED STENCILS:
The step stencil technology allows varying the stencil thickness within one stencil - thin and thick stencil areas can be combined. This technology is able to supply the right amount of solder volume to each component.

Material can be removed form squeegee or substrate side of the stencil. Cavities can be built into the substrate side to compensate non flat or sensitive areas of the substrate, like to height solder resist, to height via filling / plugging, labels or over top clamping. Please refer to section stencil cavities.
Limitations are just coming from the ability of the squeegee to follow the height profile of the stencil surface. Therefore tables indicating the required distances are available to implement the required space into the layout (refer to table below).

Table 1. Step height and dimensions.

Step Height (t)	Distance (c; d)	Step Length (a)	Step Width (b)
10 µm	>0,3 mm	>0,3 mm	>0,3 mm
30 µm	>0,9 mm	>1,5 mm	>1,5 mm
50 µm	>1,7 mm	>10,0 mm	>2,0 mm
100 µm	>5,8 mm	>30,0 mm	>10,0 mm
250 µm	>12,0 mm	>75,0 mm	>10,0 mm

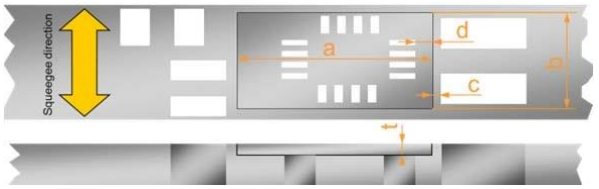

Figure 5. Design rules for step stencils.
With stepped stencils it is possible to have base thickness of e. g. 120 µm, a fine pitch area with a step down to 100 µm together with a step up to 180 µm for a connector with a coplanarity issue.

STENCIL CAVITIES:
Cavities in a stencil provide the ability to compensate peaks or objects rising above the pad level of the substrate. This helps to establish a good sealing between stencil and pad surface and prevents extensive cleaning and poor print quality.

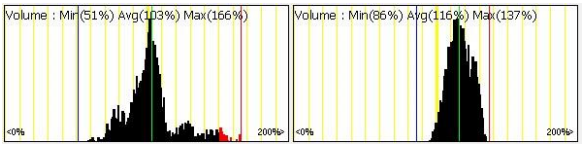

Figure 6. Volume deviation of a printed PCB. Left: no cavity for the overtop clamping; right: with cavity

Cavities typically use up to half the local stencil thickness to generate room for substrate peaks. Under certain conditions up to 80 % of the stencil thickness can be used to form a cavity.

Typical issues which implement the use of cavities are:

Filled Vias
If the via filling is higher as the pad level of the substrate it will cause a stand-off of the stencil in its surrounding area. If stencil openings are located in its proximity they will show stronger a tendency to solder paste bridging.
Vias can be compensated with a cylindrical cavity.

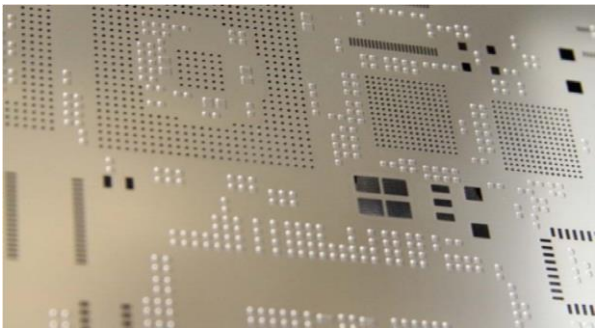

Figure 7. Via cavities in the substrate side of a stencil.

Labels
Often labels have to be placed on substrates do clearly identify the product. Normal labels have a thickness of (50

… 150) µm. This height will lead to serious printing issues if located in a distance < 6 mm to a pad. Often not the complete height of the label can be compensated with a cavity, because the stencil is often thinner as the label itself, but by reducing the effective height of the label with a cavity the critical distance to pads will be reduced.

Overtop Clamping

Many solder paste printers are using overtop clamping to fix the substrate during the printing process. The thin metal blades used for the clamping typically have a thickness of (100 … 150) µm. This will lead to the same issues mentioned above for labels.

Solder Mask

The solder resist height should not exceed the pad height, but due to required electrical parameters the thickness of solder resist may vary. If the solder resist height is higher as the pad height it will lead to printing issues for fine pitch components and delicate stencil openings. The additional stand-off will add more solder paste volume to the pad and also a sealing between stencil and pad does not exist. Therefore bridging may occur and more cleaning action is needed. Cavities around the openings on the substrate side of the stencil are providing the capability to dive into a solder resist window and set the stencil directly on the pads to compensate the negative effects of the too high solder resist.

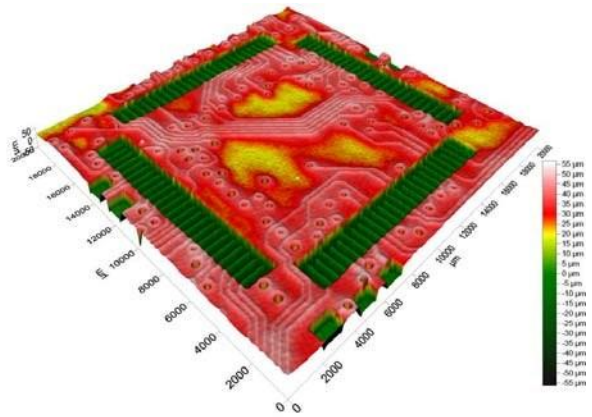

Figure 8. Height plot of the landing area for a pitch 0,4 mm QFP. Due to electrical reasons solder resist was applied two times, what made printing impossible. The zero level is colored green (all pads). All elevations above 25 µm (solder resist) are red. The heighest peaks are white. Maximum peak is 55 µm over pad level.

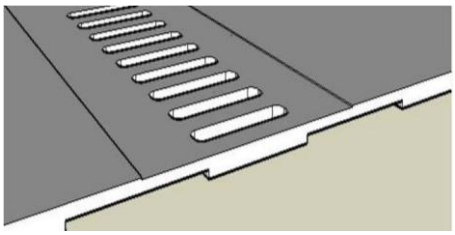

Figure 9. Solution for the issue of figure 8: The substrate side of the stencil has caities around the apertures, which allow the stencil to dive into the solder resist opening. For further volume reduction the stencil was also thinned from the squeegee side.

Printed Depots

Certain processes need two separately performed printing steps. Two stencil printers in a row or a second pass through the same stencil printer with a different stencil can be used. This technology enables to print two different materials (e. g. solder paste and glue) or to print different heights of one material with different stencil thicknesses. In these cases the layer with the lowest wet height is printed fist. The second stencil is typically thicker as the first stencil and has cavities to assimilate the already printed deposits without touching them.

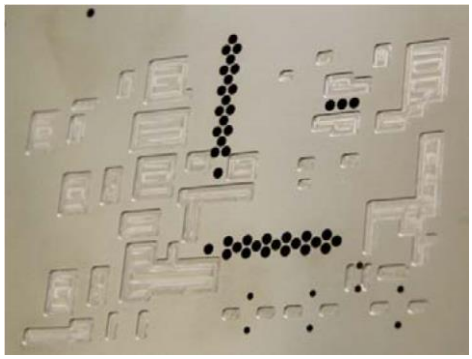

Figure 10. Stencil with cavities for already printed solder paste depots on the PCB. The round openings are used for the second print step.

Components And Masking Films

Sometimes substrates have already components placed or masking films covering sensitive areas of the substrate before they will be printed. Also parts or pins of other components could be peaking through the surface of the substrate and interfere with the printing task. In these cases cavities will help to enable a printing process.

Often components or masking films easily exceed heights of more than a millimeter. To be able to run the squeegee blade over such high differences and be able to print the area around such objects specialized squeegees are needed. For such tasks the squeegee will get fine laser cuts to allow a free movement of it sections. The shape of these squeegees will be more detailed explained in the next section.

3-D-STENCILS:

Stencils which allow printing on separated substrate height levels are called 3-D-stencils. The demand for such stencils is driven by components with their contacts on separate height levels and by substrates which have height differences between their populated areas [2; 3].

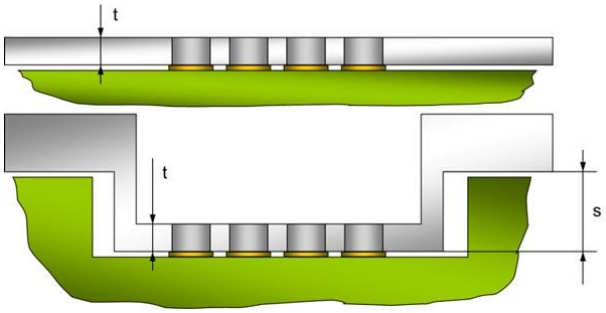

Figure 11. 3-D-Stencils are able to print into cavities of the substrate. Simultaneous printing on different height levels is also possible.

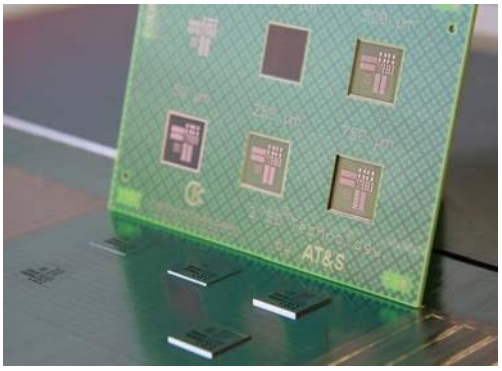

Figure 12. AT&S substrate with five different print levels (0 … 750) µm and the fitting stencil – seen form the substrate side.

In the paste a dispenser had to be used to transfer the solder paste to the non-flat areas. What would lead to extended cycle times, compaction of solder particles in needles and investing into new equipment.

3-D-Stencils have one or more thicknesses shifted on certain print levels. The design of stencil and squeegee is quite complex but give the ability to use a standard stencil printer for these kind of application.

Transferring A Layout From 2-D Into 3-D

First the required paste height for the different areas of the substrate has to be set, to be able to calculate the step height for the squeegee. Out of these values the room around the pads needed for stencil walls, tolerances and squeegee behavior during printing is calculated. Typically the stencil

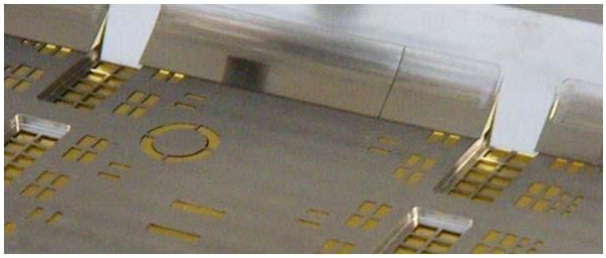

Figure 13. Sectioned squeegee printing simultaneously on two print levels.

supplier will advise theses values during the design phase of the product.

The squeegee for the 3-D-stencil is designed to print as a normal squeegee on the flat areas of the stencil and to dive into or lift over steps of up to 1,6 mm. Therefore sections suiting to the step design of the stencil will be made to give the squeegee the ability to adapt to the stencil shape. Huge height differences will limit the squeegee lifetime due to the strong deflection of the sections.

PLASMA STENCIL:

An electro polished aperture wall and substrate side of a stencil is able to enhance the paste release and provide an easy cleaning process. Especially for fine pitch structures this is very useful.

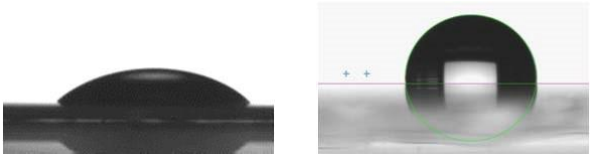

Figure 14. Contact angle on stainless steel (left) and PLASMA coated stainless steel (right).

An additional coating will advance the surface energy to increase the positive effect for the paste release. The higher surface energy will lower the bridging effect during printing, leading to extended intervals between the under stencil cleaner (USC) wipes. Also the effect of substrate tolerances such as pad size, solder resist height is reduced. This concludes to a higher throughput and a more constant paste volume – due to the reduce amount of restarts after cleaning.

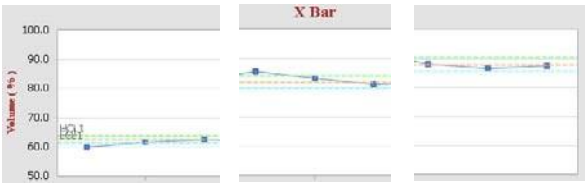

Figure 15. Percental volume transfer of a 0201 aperture for laser cut (left), laser cut & electro polished (middle) and PLASMA coated (right).

CONCLUSION:

Stencil technology is the key to establish a reliable and cost effective printing process.

Efficiency and yield will increase together with the correct selection of layout and stencil options to meet the demands of the process. To select the right combination of options a good communication between production and stencil design is essential.

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