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Reliability Evaluation of One-Pass and Two-Pass Techniques of Assembly for Package on Packages under Torsion Loads

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ABSTRACT
Package on Packages (PoP) find use in applications that require high performance with increased memory density. One of the greatest benefits of PoP technology is the elimination of the expensive and challenging task of routing high-speed memory lines from under the processor chip out to memory chip in separate packages. Instead, the memory sits on top of the processor and the connections are automatically made during assembly. For this reason PoP technology has gained wide acceptance in cell phones and other mobile applications. PoP technology can be assembled using one-pass and two-pass assembly processes. In the one-pass technique the processor is first mounted to the board, the memory is mounted to the processor and the finished board is then run through the reflow oven in a single pass. The two-pass technique has an intermediate step in which the memory is first mounted onto the processor. Then, these two parts are placed in a carrier tray and reflowed. These joined devices are then mounted on the circuit board and the finished board is reflowed a second time. The two-pass technique has a distinct advantage in that the PoPs can be checked for defects before final assembly using a non-destructive test (such as X-Ray) and hence one would expect higher yield. For this study, identical test vehicles were assembled with eight PoP packages assembled with SAC105 and SAC125 solder for the bottom BGA and top BGA respectively. One-pass technique and two-pass technique were used to assemble two test vehicles each. These test vehicles were evaluated under mechanical torsion loading to establish if method of assembly used has any impact on the mechanical fatigue durability. This was followed by failure analysis to determine failure sites. Time to failure data was plotted as Weibull 2-parameter distributions and ANOVA analysis was performed. No statistically significant difference was found in the reliability of the packages assembled using the two different techniques.

KEYWORD: Assembly techniques, Package on packages, Lead-free solders, Torsion loading, Reliability assessment, E-SEM, ANOVA, Dye and Pry technique.

INTRODUCTION:
Package on package (PoP) technology involves vertical stacking of two or more packages to allow better density. PoP configurations conventionally involve stacked memory chips or integrated memory and logic chips. Memory chips conventionally require fewer IOs when compared to logic chips. For this reason standard configurations involve a low pitch (high density) package with processor on the bottom package and the higher pitch (low density) package with the memory chips (stacked or otherwise) on the top package. Ball grid array (BGA) packages are conventionally used in PoP applications due to their high IO density and reliability [1, **Error! Reference source not found.**]. A schematic of a conventional package on package is shown in **Error! Reference source not found.**.

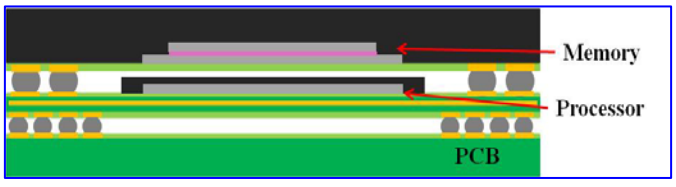

Figure 1: Package on package technology

Some of the obvious advantages of package on package technology are more efficient utilization of board space, easier routing and lower transmission time between processor and memory chips, better electrical performance with lower noise [1]. And this can be achieved using only “known good” packages since the memory and logic packages can be tested separately

and then assembled, unlike in chip scaled packages. PoP technology has gained quick acceptance in the cell phone and mobile computing market [4].

Package on packages can be assembled using two techniques, one pass technique and two pass technique. The one pass technique involves screen printing the printed wiring assembly (PWA) and then placing the bottom BGA package. This is followed by dipping the top BGA package and stacking on the bottom BGA package. Then, using a single reflow, the package is assembled. A schematic of this process is shown in **Error! Reference source not found.**. This method has an advantage that the memory and logic chip can be used exclusively and provides more logistic flexibility [5].

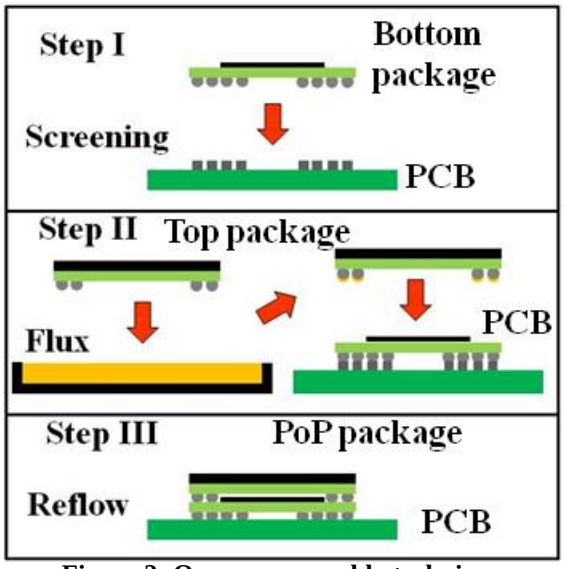

Figure 2: One pass assembly technique

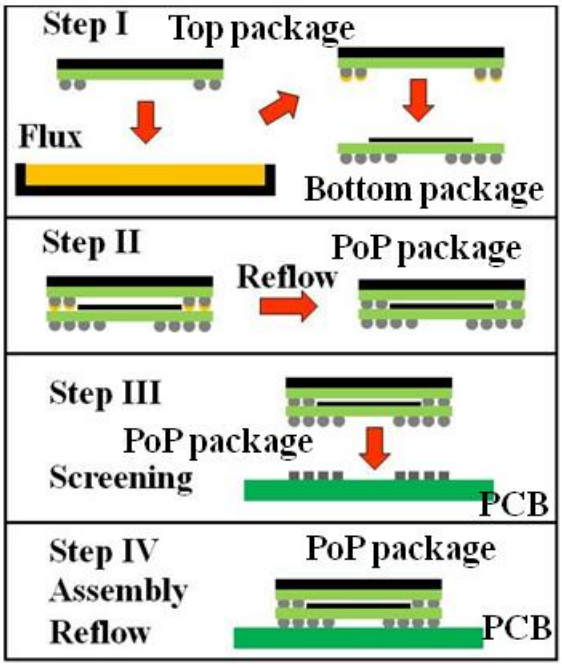

Figure 3: Two pass assembly technique

The two pass technique involves dipping the top package in flux and stacking on the bottom package on the carrier tray. At this point the package is reflowed once to make the solder connections between the top and bottom package. This is followed by screen printing the PWA and placing the stacked package on package followed by the second reflow process to make the solder interconnects between board and package. A schematic representation of this process is shown in **Error! Reference source not found.**.

This technique allows us to introduce another quality control check after stacking of packages using non-destructive test methods such as X-ray. An example of such non destructive testing using X-Ray is shown in **Error! Reference source not found.**. This ensures better board yields since defects in interconnect between top and bottom BGA can be screened before final assembly on the PWA [6].

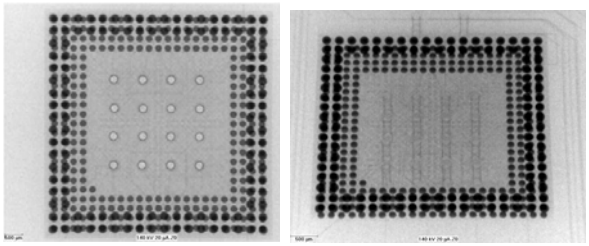

Figure 5: X-Ray of PoP technology

The standardization concerning the package outline drawings specific to bottom package [7, 8] and top package pin out configuration as described by JEDEC. However, from a reliability perspective, available literature largely discusses drop testing [9-9] and a few studies have addressed thermal reliability [2, 6, 11-13]. Also, the warpage during reflow has been characterized [14-17]. However, printed wiring assemblies in cell phones and mobile computing often encounter other types of mechanical loads such as vibration, bend and torsion. Also, no literature is available to compare the reliability performance of PoP technology when assembled using two different techniques.
Mechanical torsion test involves replicating loading on PWA in life where transverse adjacent loads cause shear loading of second level interconnects. Mechanical Torsion in literature have been used to evaluate the reliability of voids in Plastic Ball Grid Arrays [18], evaluation of lead-free solders [19], comparing different surface finished on copper [20] and to evaluate reballing and solder paste volume's impact on reliability [21]. Torsion tests are also used to simulate loads commonly experienced by laptop printed wiring boards [22] and cell phone [23]. Currently, there is no accepted standardize test procedure for MDS or torsion based testing.

This study discusses the board level reliability of PoP technology under mechanical torsion loads. The impact of assembly technique used and its impact on reliability are discussed. Also, the impact of solder paste selection on the bottom package was examined. Also, statistical analysis was performed on the failed samples to determine failure sites and relevant failure mechanisms. An assessment in the distribution of failure sites was performed to ascertain that the performance and nature failures do not vary with assembly technique. The following section will include details on the test vehicles. This is followed by a description of test setup. Then, the results are reported with relevant failure analysis. Finally, the conclusions of the study are presented.

TEST VEHICLE:
The test vehicle used in this study consists of PWA of the dimension, 8″ × 4.5″ × 62 mils. The PWA cards were built using Polyclad 370HR board laminate with OSP board finish. Eight PoP packages were assembled into two clusters with quarter board symmetry. Package dimensions of 12×12 mm were selected with package laminate of 0.21 mm. The top package in the configuration consisted of a peripheral BGA package of 0.65 mm pitch with 128 pads in a 18×18 ball matrix. The bottom package used a peripheral BGA package with 0.5 mm pitch and 305 pads in a 23×23 ball matrix. The packages in the outer cluster are referred to as stress level I and the inner cluster as stress level II. The strains observed at stress level II are marginally higher than stress level I and hence one can expect components placed at stress level I to last longer than components at stress level II. The test vehicle with the stress levels marked is shown in **Error! Reference source not found.**.

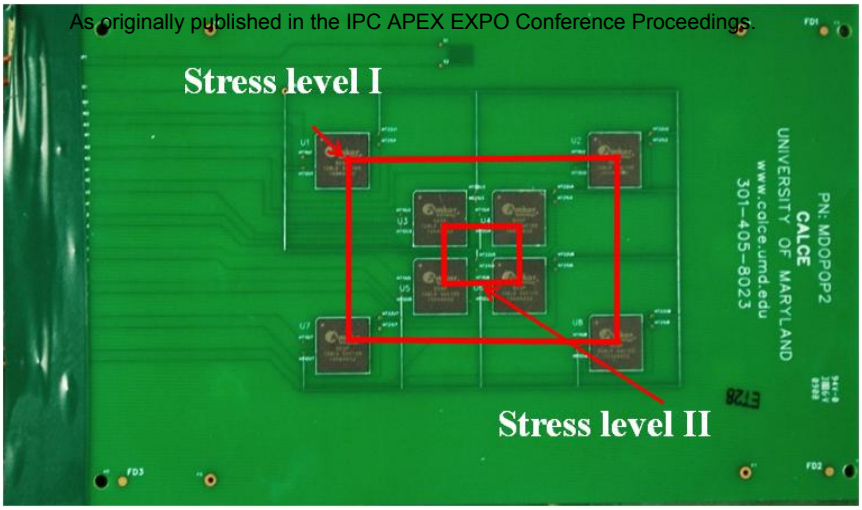

Figure 6: Test Vehicle

The PoP components used had three daisy chain nets to allow continuous resistance monitoring during test. The corner 12 solder balls of the top package formed the first daisy chain, while the remaining solder balls in the top package formed the second daisy chain. Two daisy chains were used for the top package and a single daisy chain for solder balls on the bottom package. This was done to identify the net of solder balls to experience the first failure in the package.

Test vehicles were assembled using the two assembly techniques discussed in the introduction section. The solder pastes used to assemble the top BGA package was SAC105 (98.5%Sn + 1.0%Ag + 0.5Cu) in all test vehicles. This was chosen because the top package is susceptible to drop loading and literature strongly suggests that SAC105 has better shock durability when compared to other high silver solders. The bottom package was expected to experience more fatigue loading and hence the bottom BGA package was assembled using SAC125 (98.3%Sn + 1.2%Ag + 0.5%Cu) or SAC305 (96.5%Sn + 3.0%Ag + 0.5%Cu).

The test matrix consists of test vehicles assembled using one-pass assembly technique and two pass technique with SAC105 and SAC125 solder paste combination for the top and bottom packages respectively (with a sample space of 2 test vehicles). Also, two test vehicles assembled using one pass method but with SAC305 solder paste used to assemble the bottom package.

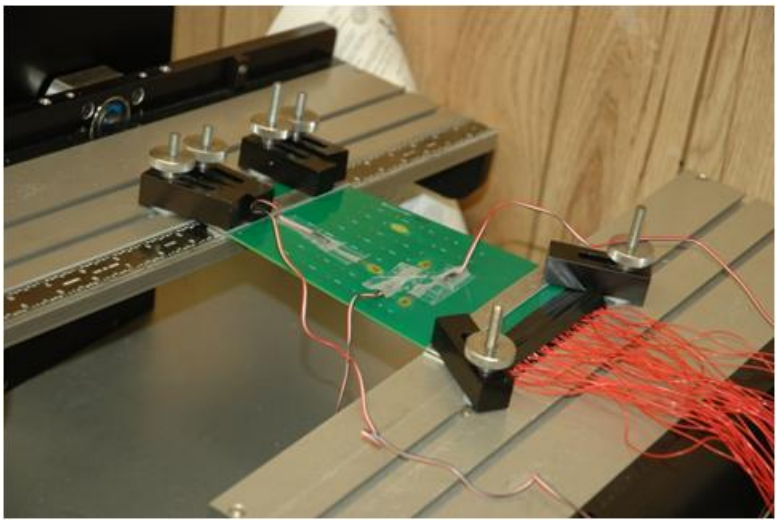

Figure 7: Test setup

Table 1: Test Matrix

Board Type	Solder Alloy	Tested
Pre-PoP board	SAC125(base) and SAC105(top)	2
PoP Boards	SAC125(base) and SAC105(top)	2
PoP305 Boards	SAC305(base) and SAC105(top)	2

In this study the one pass assembled packages will be referred to as "PoPxxx" while the two pass assembled packages will be referred to as "PrePoPxxx", where the xxx is used to describe the solder composition of the bottom package. For instance, PrePoP125 refers to a two-pass assembled package, with SAC105 solder on the top package and SAC125 solder on the bottom package, while PoP305 would refer to a one pass assembled package with SAC105 on top package and SAC305 solder paste on the bottom package.

TEST SETUP:
The test setup involves use of a static platform and rotary platform to introduce torsion loads on the PWA. The rotary platform has controlled rotary displacement with ability to define angular displacement, angular velocity and angular acceleration with feedback. The thickness of the PWA is also taken into consideration and necessary changes are made to ensure that the axis of rotation passes through the center of the PWA. This allows us to control peak-to-peak board strain and average strain rate. An angular deflection of 4.5° full cyclic load was selected at angular velocity of 1°/s and angular acceleration of $1°/s^2$. This approximately translates into board shear strain of 1000 µstrain units at an average strain rate of 50 µstrain units/sec. Preliminary finite element analysis work performed on the test setup has been explained in previous work [24].

However, for valid results test variables will be compared only within the same stress level. Also, the failure criteria used for this study is based on IPC-9701 [25]. A 20% increase in nominal resistance for 5 successive cycles was defined as failure. Also, considering the nature of configuration of the package, irrespective of failure of memory or logic IOs the functionality of the package is affected. Hence, the first failure of any of the three nets was defined as failure in this study.

All test vehicles were cycled to 100% failure. Two strain gages were pasted on each vehicle adjacent to PoP component at stress level I and II. This was performed to compare strain loads and also as reference for future finite element analysis work.

RESULTS
The resistances of all the daisy chain nets were monitored and cycles to failure data was obtained. The failure data was then plotted assuming a Weibull 2-parameter distribution. Data was grouped based on the placement (stress level) of the packages. Test results at stress level I are shown in **Error! Reference source not found.**. ANOVA analysis was performed on the test results and no statistically significant difference was observable between the one pass and two pass assembly techniques. Also no difference in performance was observable between the PoP components assembled with SAC125 and SAC305 solder pastes for the bottom package. This suggests that the increased stiffness due to stacking of the packages has increased the solder strain on the bottom package. This will be confirmed using finite element analysis. The trends are consistent at stress level II too as seen in **Error! Reference source not found.**.

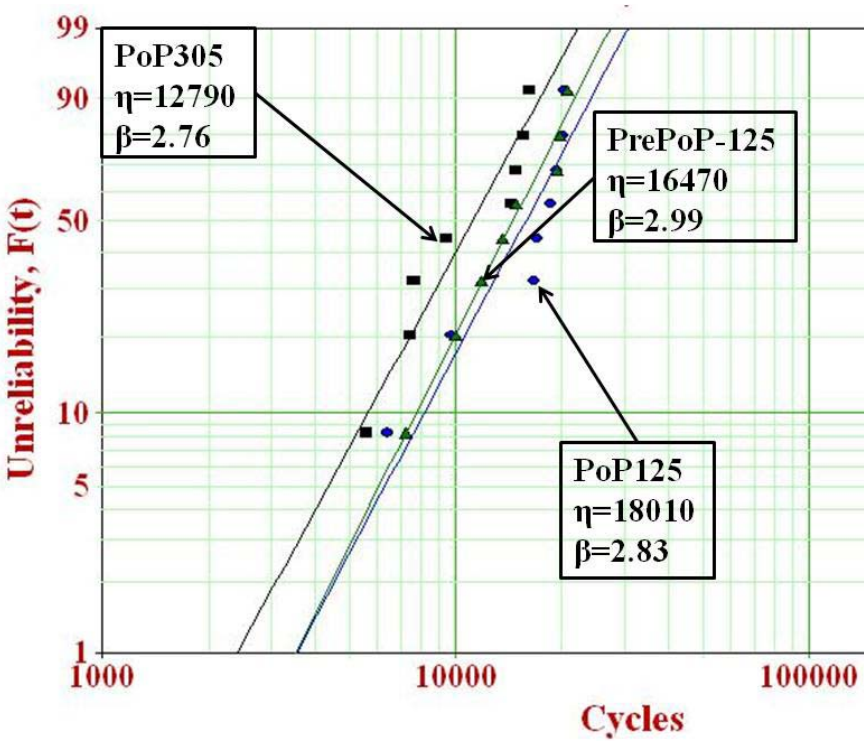

Figure 8: Weibull Analysis- Stress Level I

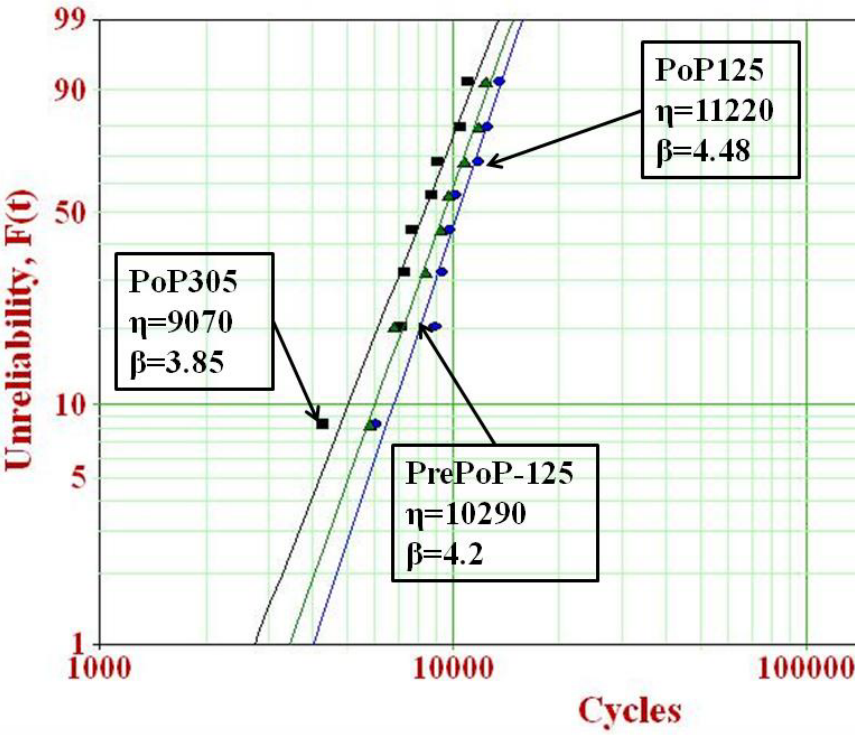

Figure 9: Weibull Analysis- Stress Level II

Another interesting observation was that all the first failures on the packages were observed on the daisy chain net of the bottom package. This suggests that the solder strain is maximum at the solder joints on the bottom packages.

FAILURE ANALYSIS

The resistance monitoring showed that the first failures were on the bottom packages. Destructive failure analysis was performed to determine the failure site and compare between test vehicles. **Error! Reference source not found.** shows an E-SEM image of a PoP125 component from stress level I.

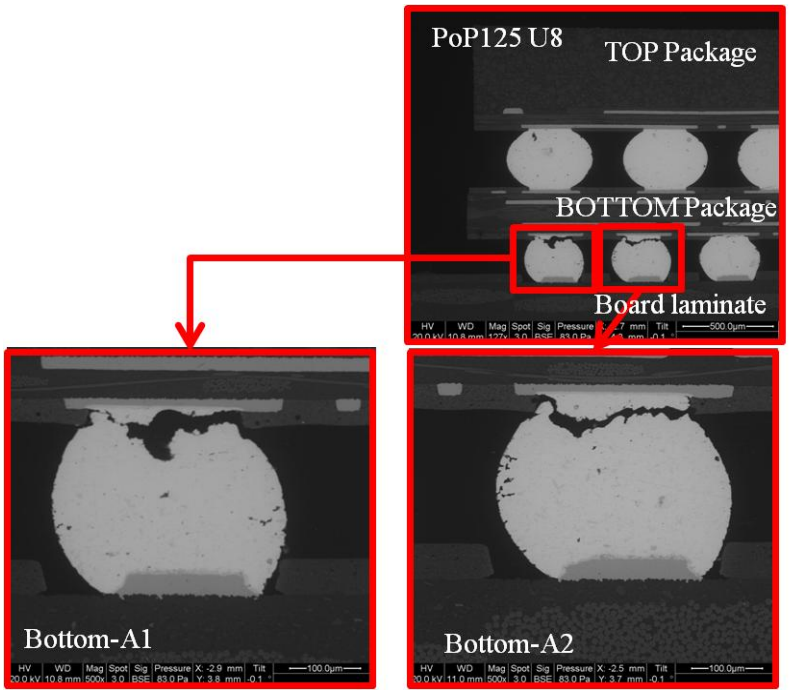

Figure 10: E-SEM image of cross sections of PoP125

The test vehicle was tested for 18200 cycles and the package shown in **Error! Reference source not found.** failed at 6399 cycles. All interconnect failures were observed on the bottom package's second level interconnects. Cracks were located on the package-solder interface. Also, several instances of pad cratering were observed. Similar observations were made in the PoP305 package at stress level I. An instance of pad cratering observed under E-SEM has been shown in **Error! Reference source not found.**. Similar observations were made on the PrePoP-125 package.

Pad cratering is defined as cracking in the thin resin rich region underneath the copper pads and traces [26]. Literature classifies the crack mechanisms commonly observed into the following two categories, cohesive failure and. adhesive failure. Fracture that occurs along the resin region alone is referred to as cohesive failure, while fracture between the resin and glass fiber bundles is called adhesive failure. All instances of pad cratering in this study were cohesive failures. Pad cratering by itself does not refer to an electrical failure of solder joints or the loss of functionality of package. However, the crack in the resin may result in failures on the connecting trace on the PWA, and thus cause an electrical open. However, even if the trace is not severed, or the pad is non-functional, a crack in the underlying laminate is a source of reliability concern [27]. Use of underfill is suggested as a mitigation technique [28].

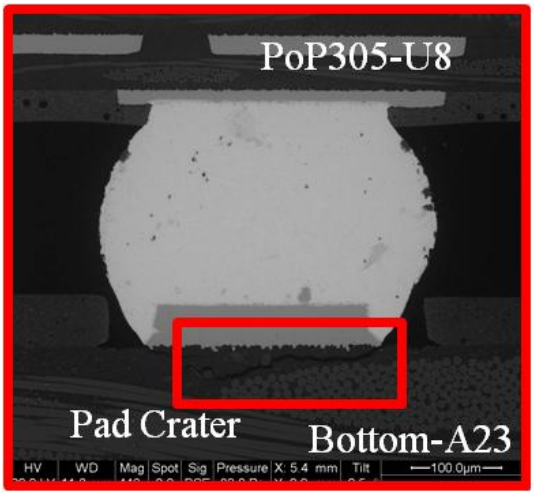

Figure 11: E-SEM image of pad cratering observed in PoP305 at stress level I

However, the objective of the study is to compare if the selection of assembly technique has an impact on reliability of the PoP assembly. Hence, to understand the failure site distribution and compare between assembly techniques and solder selection, dye and pry of components was performed and different failure site distribution was compared. This was followed by documentation of number of instances of each failure site and normalization to allow easy comparison.

Results from this study are shown in **Error! Reference source not found.** and **Error! Reference source not found.**. It is clear that no statistically significant change in distribution occurs with change in assembly techniques. Also, change in solder paste does not impact the failure site either. Since the components were tested to first failure of the three nets, the number of balls on the top package in PoP assembly with no failure is high. We also do not observe any instances of pad cratering or trace failure on the intermediate laminate but instead only the PWA. Component- solder interface is the most common failure site observed on all samples.

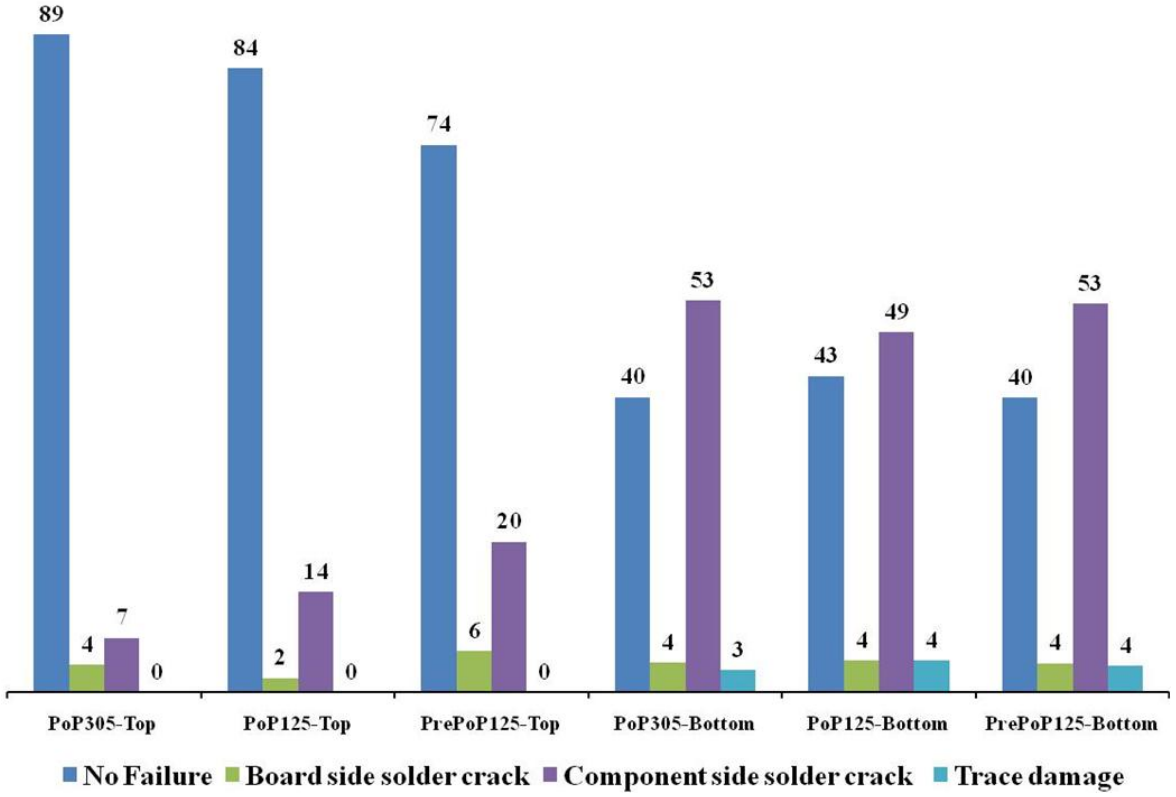

Figure 12: Dye & Pry Results, Stress Level I (Normalized)

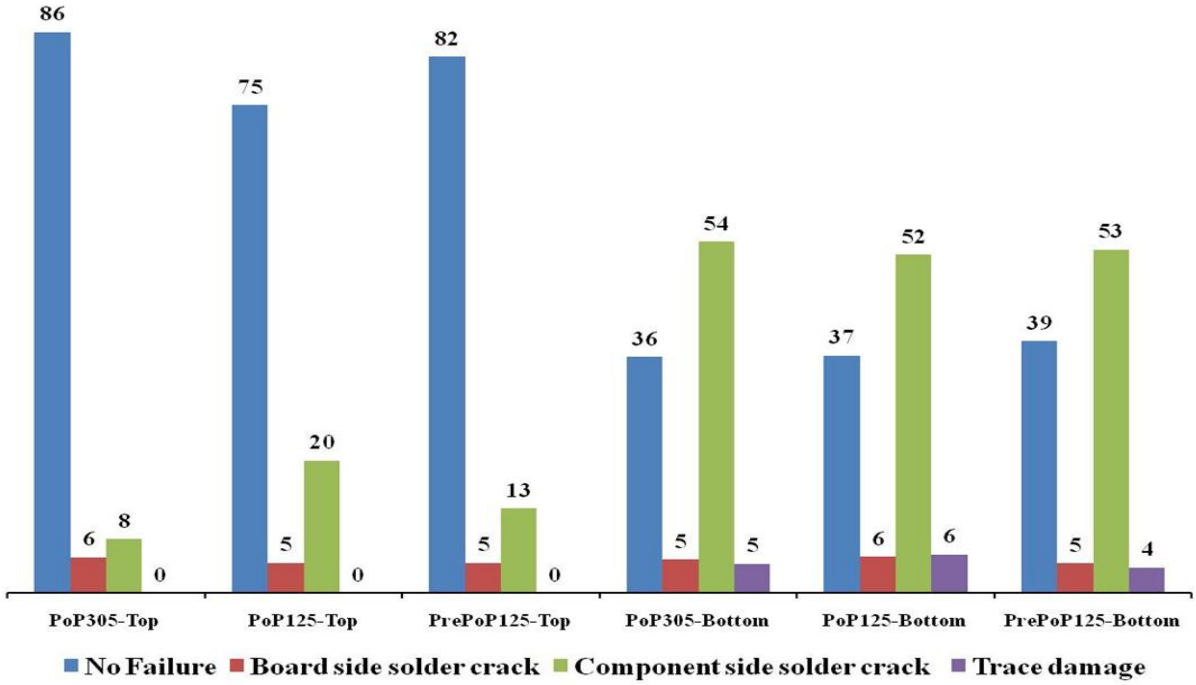

Figure 13: Dye & Pry Results, Stress Level II (Normalized)

CONCLUSIONS

Mechanical torsion loading was used to compare the different assembly techniques for package on package technology and no statistically significant difference was observed. The bottom nets were always found to fail first in PoP assemblies. No statistically significant difference in durability was observed for PoP technology with increased Ag content in the solder interconnects of bottom package under mechanical torsion. No difference in trend of failure distribution was observed between solder types or assembly techniques for package on packages. Pad cratering was identified to be a potential reliability concern. Use of under fill is recommended to redistribute stress uniformly and avoid trace failures.

REFERENCES

1. Carson, F., "POP Developments and Trends," Proceedings IMAPs Device Packaging Conf, Scottsdale, AZ, Mar. 2006.
2. Lenihan, T.G., Jan Vardaman, E., "Worldwide Perspectives on SiP Markets: Technology Trends and Challenges", ICEPT '06. 7th International Conference on Electronic Packaging Technology, vol., no., pp.1-3, 26-29 Aug. 2006.
3. Menon, A.R., Karajgikar, S., Agonafer, D., "Thermal design optimization of a package on package" Semiconductor Thermal Measurement and Management Symposium, SEMI-THERM 2009. 25th Annual IEEE, vol., no., pp.329-335, 15-19 Mar. 2009.
4. Kada, M. and Smith, L., “Advancements in Stacked Chip Scale Packaging (S-CSP) Provides System in a Package Functionality for Wireless and Handheld Applications,” Pan Pacific Microelectronics Symposium, 2000.
5. Sjoberg, J.; Geiger, D.A., Shangguan, D., "Process development and reliability evaluation for inline Package-on-Package (pop) assembly", Electronic Components and Technology Conference. ECTC 2008. 58th, vol., no., pp.2005-2010, 27-30 May 2008.
6. McCormick, H., Sterian, I., Chow, J., Berry, M., Trudell, J., and Cortero, R., “PoP: An EMS perspective on assembly, rework and reliability”, SMTA Pan Pacific, vol. 9, no., 3, Feb. 10 - 12, 2009.
7. JEDEC JC-11 Committee, JEDEC design standard design requirements for outlines of solid state and related products, JEDEC publication 95, Design guide 4.2.
8. Dreiza, M., et al., "Stacked Package-on-Package Design Guidelines", International Wafer Level Packaging conference, 2005.
9. Jing-en Luan, "Design for Improvement of Drop Impact Performance of Package-on Package", Electronics Packaging Technology Conference. EPTC 2007. 9th, vol., no., pp.937-942, 10-12 Dec. 2007.
10. Lai, Yi-Shao, Yeh, Chang-Lin, Wang, Ching-Chun, “Examination of board-level drop reliability of package-on-package stacking assemblies of different structural configurations”, Microelectronic Engineering, vol. 84, no. 1, pp. 87-94, Jan 2007.
11. Wang, V., Maslyk, D., "Analysis of the reliability of package-on-package devices manufactured using various underfill methods," ICEPT-HDP 2008. International Conference on Electronic Packaging Technology & High Density Packaging, vol., no., pp.1-3, 28-31 Jul. 2008.
12. Lee, Joon-Yeob, Hwang, Tae-Kyung, Kim, Jin-Young, Min Yoo, Sohn, Eun-Sook, Chung, Ji-Young, Dreiza, M., "Study on the Board Level Reliability Test of Package on Package (PoP) with 2nd Level Underfill,"Electronic Components and Technology Conference,. ECTC '07. Proceedings. 57th, vol., no., pp.1905-1910, 29, May- 1, Jun. 2007.
13. Hwang, Tae Kyung, Sohn, Eun Sook, Kang, Won Joon, Cha, Se Woong, Lee, Joon Yeob, Hwang, Chan Ha, Lee, Choon Heung, "Board level reliability assessments of package on package", EMAP 2007. International Conference on Electronic Materials and Packaging, vol., no., pp.1-7, 19-22 Nov. 2007.
14. Vijayaragavan, N.; Carson, F.; Mistry, A., "Package on Package warpage - impact on surface mount yields and board level reliability,"Electronic Components and Technology Conference, ECTC 2008. 58th, vol., no., pp.389-396, 27-30 May 2008.
15. Zhao, J, Luo, Y., Huang, Z., Ma, R., "Effects of package design on top PoP package warpage", Electronic Components and Technology Conference, ECTC 2008. 58th, vol., no., pp.1082-1088, 27-30 May 2008.
16. Carson, F.; Seong Min Lee; Vijayaragavan, N., "Controlling Top Package Warpage for POP Applications", Electronic Components and Technology Conference, ECTC '07. Proceedings. 57th, vol., no., pp.737-742, May 29 2007-June 1 2007.
17. Hao Tang; Nguyen, J.; Zhang, J.; Chien, I., "Warpage Study of a Package on Package Configuration,", HDP '07. International Symposium on High Density packaging and Microsystem Integration, vol., no., pp.1-5, 26-28 June 2007.

18. Yunus, M.; Primavera, A.; Srihari, K.; Pitarresi, J.M., "Effect of voids on the reliability of BGA/CSP solder joints," Electronics Manufacturing Technology Symposium, Twenty-Sixth IEEE/CPMT International , vol., no., pp.207-213, 2000.
19. Ryan, C.; Punch, J.; Rodgers, B., "A reliability evaluation of lead-free ball grid array (BGA) solder joints through mechanical fatigue testing,", EuroSimE 2005. Proceedings of the 6th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Micro-Electronics and Micro-Systems, vol., no., pp. 436-440, 18-20 April 2005.
20. Yee, S., Ladhar, H., "Reliability comparison of different surface finishes on copper," Circuit World, vol., no., 25 no.1, pp. 25-29, 1999.
21. Maia Filho, W.C.; Brizoux, M.; Fremont, H.; Danto, Y.,"Torsion test applied for reballing and solder paste volume evaluation," 18th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis Microelectronics reliability , vol. 47, no. 9-11, pp. 1663-1667, Sept.-Nov. 2007.
22. Haiyu Qi; Qian Zhang; Tinsley, E.C.; Osterman, M.; Pecht, M.G., "High Cycle Cyclic Torsion Fatigue of PBGA Pb-Free Solder Joints," IEEE Transactions on Components and Packaging Technologies, vol.31, no.2, pp.309-314, Jun. 2008.
23. Kunal Goray, “Durability of Surface Mount Assemblies Under Flexural Loads”, MS Thesis, University of Maryland, College Park, 2001.
24. Srinivas, V., Al-Bassyiouni, M., Osterman, M., Pecht, M., “Characterization of lead-free solder interconnects reliability under torsional loads”, ASME International Mechanical Engineering Congress and Exposition, 2009.
25. IPC, IPC-9701 “Performance Test Methods and Qualification Requirements for Surface mount Solder Attachments”, IL, Jan, 2002.
26. C.F. Coombs, Printed circuits handbook, McGraw-Hill (2001).
27. Roggeman, B.; Borgesen, P.; Jing Li; Godbole, G.; Tumne, P.; Srihari, K.; Levo, T.; Pitarresi, J., "Assessment of PCB pad cratering resistance by joint level testing," Electronic Components and Technology Conference, ECTC 2008. 58th , vol., no., pp.884-892, 27-30 May 2008.
28. Schueller, R., Ables, W., and Fitch, J. “A Case Study for Transitioning Class A Server Motherboards to Lead-Free”, SMTA International, August 2008.