

Assembly and Reliability Investigation of Package on Package

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Abstract

This paper discusses the results of several independent experiments designed to address the many aspects of successful PoP integration. Assembly through the use of in-line stacking and pre-stacking was evaluated. Top package soldering was performed by dipping in either flux or paste. The warpage behavior of each level, as well as the full module was characterized through simulated reflow using Shadow-Moiré analysis. Warpage behavior was found to be a limiting factor in assembly yields.

Reliability of PoP assemblies was evaluated using drop/shock, vibration and thermal cycling. The level at which failure occurred depended on the location of the module on the PCB. Underfill was found to greatly enhance mechanical reliability, however thermal cycling reliability was decreased.

Introduction

Package on Package (PoP) was developed to integrate the logic and memory devices primarily found in portable consumer products. Stacking the devices allows for vertical expansion while minimizing overall footprint. Several levels of stacking might be used, and the assembly and reliability consequences are not trivial.

Assembly yields will be greatly affected by the individual package characteristics, including warpage, as well as the particular assembly process that is adopted. In-line stacking, where both devices are soldered in the same process step, or pre-stacking, where the module is built in a separate process step, both have their individual challenges. Further, the material selection for soldering, whether paste or flux, as well as the particular composition and even the supplier of that material, may have a drastic impact on the assembly robustness.

Reliability of PoP has so far been characterized mostly by mechanical means, as this technology is found primarily in portable and handheld electronic devices. Here, the choice of solder alloy, pad finish, and other package attributes will be critical. The complication of mechanical testing is that it is usually driven by PCB flexure, which inherently has a large location effect. Therefore it is important to characterize not only the failure rates, but the primary failure location and mode based on the location of the module on the PCB. The following summarizes several experiments intended to uncover both the assembly and reliability issues of Package-on-Package, and to help draw general conclusions that can be expanded to many other devices.

Package Warpage Characterization

Several packages were selected for characterization. These included the common 12mm and 14mm packages available from Amkor, which are made up of a PSvfBGA bottom package and an FBGA top package. In addition, 14mm and 15mm packages from other suppliers were also considered. Table 1 below summarizes the packages used in this characterization, including pad finish and solder alloy. As shown by the listing for the Amkor 12mm packages, the solder alloy and pad finish was not consistent, even for devices within the same matrix tray. Optimum reliability of non-reinforced packages was obtained when the bottom package used LFA3 solder alloy (Sn/1.2Ag/0.5Cu/0.05Ni) and Cu-OSP pads [1, 2].

Table 1. Packages selected for characterization.

Package Identifier	Body Size (mm)	Bottom Package			Top Package		
		Supplier	Pad Finish (Bottom/Top)	Solder Alloy	Supplier	Pad Finish	Solder Alloy
1	12	Amkor	Cu/ENIG	SAC305	Amkor	Cu or ENIG	SAC305 or SAC105
2	14	Amkor	Cu/ENIG	SAC305	Amkor	Cu	SAC305 or SAC105
3	14	Supplier B	ENIG/ENIG	SAC405	Supplier C	Cu	SAC305
4	15	Supplier D	NiAu/NiAu		Supplier D	NiAu	

Warpage of the two parts is critical to assembly yields [1-5]. In an in-line stacking process, where both the top and bottom packages are assembled onto the PCB at the same time, the warpage behavior of the individual levels is the critical parameter. In a pre-stacking process, the warpage of the individual packages is critical during the pre-stacking, but the behavior of the fully soldered module is important during the assembly of the module to the PCB.

The four unique PoP assemblies shown in Table 1 were measured for thermally induced warpage using an Akrometrix TherMoiré PS200 warpage measurement system. The individual packages were measured, as well as a pre-stacked module for each case. All measurements were taken on the bottom side of the packages (dead-bug orientation). The packages were heated to Pb-free reflow temperature (240 °C or 245 °C) and the surface warpage was measured at various temperatures during the profile to characterize the behavior. The sign convention from the JEDEC warpage standard [6] was adopted, which defines positive warpage as the corners of the package bending towards the PCB and negative warpage as the corners of the package bending away from the PCB (Figure 1). Figure 2 shows the warpage results for all 4 package types.

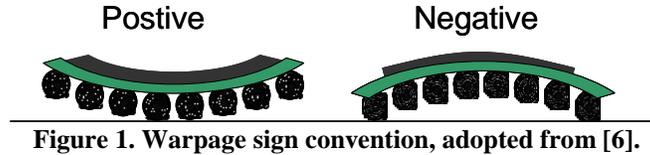


Figure 1. Warpage sign convention, adopted from [6].

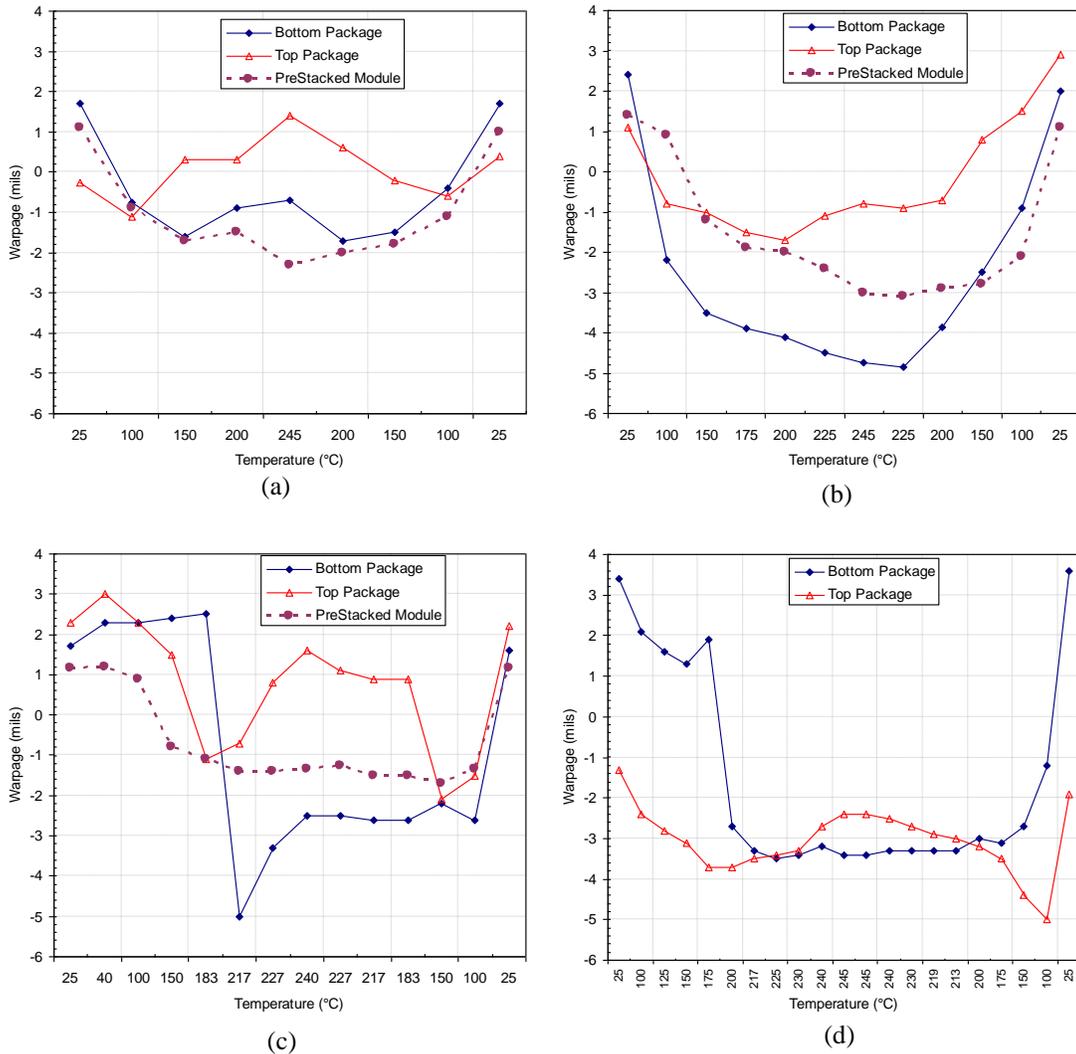


Figure 2. Warpage of different PoP Packages. (a) Amkor 12mm package; (b) Amkor 14mm package; (c) 14mm Package from Suppliers B and C; (d) 15mm Package from Supplier D.

The complex warpage characteristics of the PoP module have an impact on the solder joint formation and assembly yields. In Figure 2(a), the 12mm Amkor device does not show any surprising warpage trends, and when assembled, 100% yields were achieved whether by inline or pre-stacking the devices. Figure 2 (b) shows that the 14mm bottom package from Amkor has a high amount of negative warpage at elevated temperature, which will affect solder joint formation, discussed below. The 14mm bottom package from Supplier B had the greatest warpage change between 183 °C and 217 °C, presumably due to an unbalanced construction and exceeding the glass transition temperature of the substrate material. In the pre-stacked arrangement however, this package tends to be much more stable. The 15mm package from Supplier D shows a great amount of negative warpage at elevated temperatures, and does not relieve that warpage until past the solidification temperature of the solder. Because of this warpage behavior, the package from Supplier D exhibits many head-in-pillow failures just after assembly.

Solder Joint Formation

The 14mm Amkor PoP device was assembled onto test boards with an in-line process using both flux and paste dipping of the top package. Dip thicknesses of 30% and 50% were used for both the flux and paste dipping processes. Cross-sections were prepared after assembly, to measure solder joint heights across both the top and bottom package. Figure 3 shows the distribution of joint heights on the bottom package along an outer row of joints. This result agrees with the bottom package warpage results shown in Figure 2(b), where the corners of the package tend to warpage away from the PCB at elevated temperature, resulting in taller joints at the corners. The joint heights of the top package were more consistent along the outer row, indicating limited warping of that package relative to the bottom package. The average top package joint height as a function of dip material and thickness is shown in Figure 4. The error bars represent one standard deviation for 20 measured joints. Only the 50% flux dip was considered here, as it was assumed that flux thickness would have no effect on joint height. Paste dipping provides for 1-mil greater standoff of the top package due to the increased solder volume. We see no difference in joint height between the 30% and 50% paste dipping. The increased joint height of the top package may contribute to an overall more flexible PoP module, and the reliability consequences of this will be discussed later.

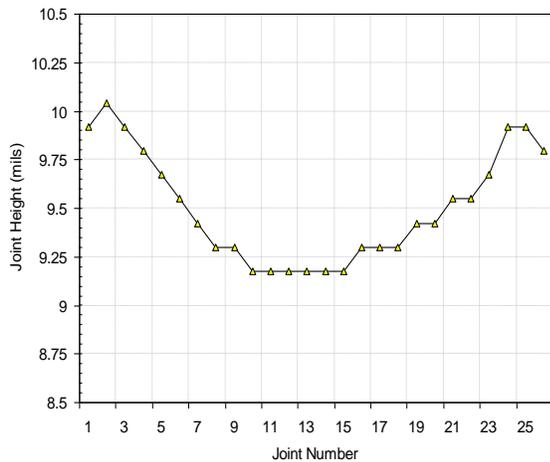


Figure 3. Solder Joint Heights along the outer row of bottom package after reflow.

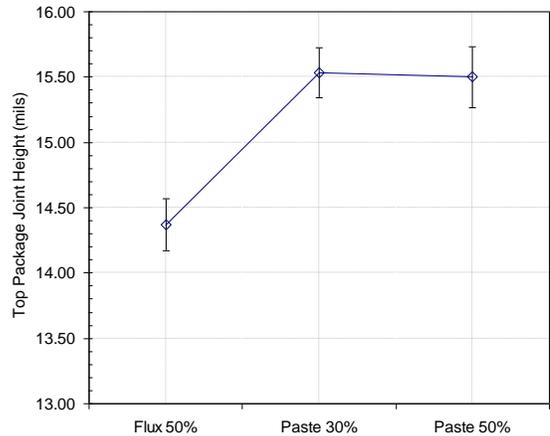


Figure 4. Solder joint heights of the top package for three dip conditions.

Pre-Stacking Assembly

An in-line assembly process for PoP is relatively straight forward using existing surface mount equipment [7]. This includes screen printing paste onto the PCB and placing the bottom packages onto the paste deposits. Top packages are then picked, dipped in flux or paste and placed onto the bottom package. No special inspection is necessary; the entire process can be performed with only global PCB fiducial recognition. Various solder paste suppliers have introduced special pastes for dipping to optimize PoP assembly.

Pre-stacking PoP modules may be desired in certain cases. Dipping the top component in flux or paste in an in-line stacking process can reduce throughput significantly compared to direct pick-and-place because of the necessary steps involved. This includes an extra ball inspection step performed after dipping to ensure that the part is not rotated by the process or lost in the flux. Some assemblers may have to invest in specialized fluxing equipment in order to assemble PoP devices and this may not be cost justifiable, so outsourcing PoP pre-stacking may be necessary. Even then, it has also been noted that some placement machines and rework stations cannot place components on top of other devices placed during the same placement program. In these cases the placement program must be terminated and a new program loaded to proceed with the process which significantly reduces throughput. Software modifications may or may not be available to correct this issue. Also, the

challenges of rework operations may be better suited to a full module replacement, which would require a pre-stacked module [8].

For the reasons listed above, a pre-stacking process was developed for the 12mm Amkor PoP package (Package ID-1). A pallet was designed containing 25 pockets in which the bottom device is loaded in the desired orientation as shown in Figure 5. Note that the loading process can easily be automated for high volume applications, but the packages were manually loaded by hand for this exercise.

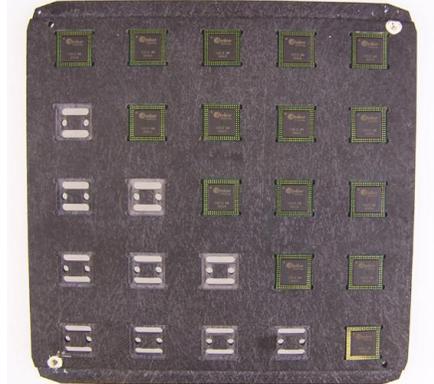


Figure 5. Stacking pallet (half loaded with PSvFBGAs).

In our case a standoff pedestal as shown in Figure 6 was included at the center of the pocket to raise the solder balls off of the bottom of the pallet. This was possible because the device is a perimeter array package. Other solder ball array types may not be able to accommodate this feature. The standoff pedestal prevents the PSvFBGA solder joints from collapsing during the initial reflow process when the top and bottom devices are joined. Flattened or coined solder balls are less desirable for the attachment process of the PoP module to the PCB. Slots were added in each pocket to optimize thermal uniformity and to reduce the thermal mass so that the oven temperatures could be lower while still providing proper soldering temperatures at the module.



Figure 6. Cross section of pallet pocket design with PSvFBGA in place.

The pallet is loaded into the pick and place machine and the locations of each component were identified by using the top surface attachment pads of the PSvFBGA as local fiducials. The top devices are picked from a feeder, dipped in flux or paste, inspected for theta correction and placed on top of the bottom packages. The entire pallet is then reflow soldered. This process was successful in creating 50 pre-stacked devices which were subsequently reflow soldered to a PCB resulting in 100% yield.

Note that the pre-stacking process was designed to compensate for component size variation by using pallet pockets which were slightly larger than the maximum size of the PoP packages based on manufacturer's tolerances. This resulted in significant "play" within each pocket and local fiducials were required to properly place the top devices. However, the actual tolerances measured were considerably smaller than published and it appears that tighter pockets could have been fabricated thereby eliminating the need for the time consuming local fiducial recognition process.

Reliability

Stackable package technology has been most widely adopted in portable and handheld electronics. Therefore the primary reliability concern is mechanical loading. Several experiments were performed to address the mechanical reliability of Package on Package devices, specifically drop and vibration reliability. Limited thermal cycling was also performed to compare PoP devices with and without underfill reinforcement. Reliability testing was only performed on the Amkor packages due to test vehicle availability.

12mm Package

Pre-stacked Amkor 12mm PoP devices were mounted onto 0.062" thick test boards, measuring 4.5x4.5 in. (114.3x114.3mm). The devices were located away from the center of the board, near the board supports shown in Figure 7. This version of the Amkor device utilized SAC305 solder joints on both levels. The pad finish on the top package was Cu, while the pad finish on the bottom package was Cu on the bottom and ENIG on the top. Drop testing was performed per JEDEC JESD22-B111 [9], with each component being electrically monitored via event detection. A total of 150 drops was recorded, with only six of eight modules failing. The characteristic life, obtained from a 2-parameter Weibull distribution was 136 drops. Notably all failures were at the top package, at the inner-most corner of the package array, closest to the board support (Figure 8). The failure mode was by cracking of the intermetallic layer at the bottom pad, as shown in Figure 9. There was also significant damage to the bottom level, in terms of pad cratering at corner pads (Figure 10). However, because the 3 corner joints in each corner are non-function mechanical pads, no electrical failure was detected.

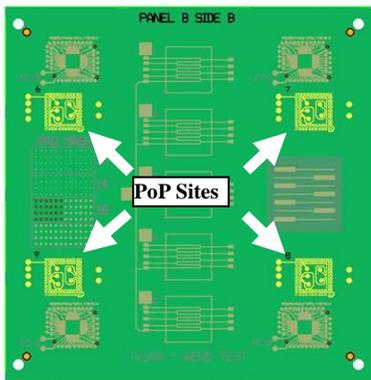


Figure 7. Diagram of test vehicle for 12mm Amkor PoP.

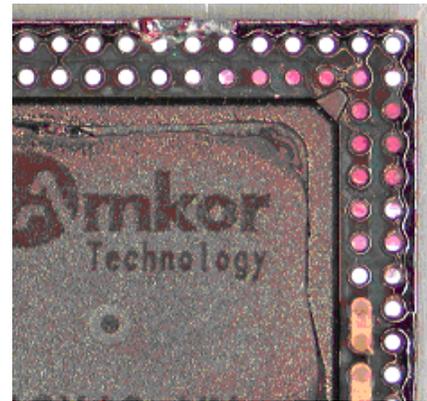


Figure 8. Failures occurred at the inner corner of the array, as shown by the red-dyed pads.

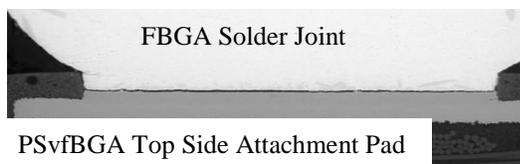


Figure 9. Cracking along through IMC at the Ni surface on the PSvFBGA.

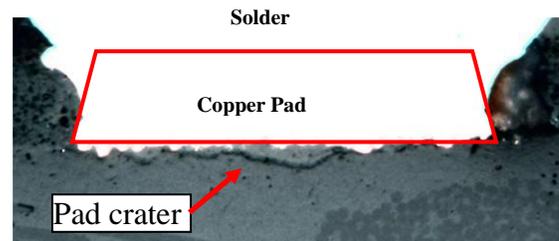


Figure 10. Pad Cratering was observed under the corner-most joints of the bottom package, but these are non-functional so no electrical failure was detected.

A second test vehicle was procured to investigate the location effect on failure modes, as well as evaluate underfill reinforcement. This second test vehicle utilized the same board dimensions as the first, but included PoP locations along the center-line of the board, where the greatest bending stresses are expected to occur during a drop event. The six PoP devices on each board were separated into two groups: Inner and Outer, as shown in Figure 11, below. This version of the 12mm Amkor package utilized ENIG pads on the top package, as opposed to Cu pads in the previous test.

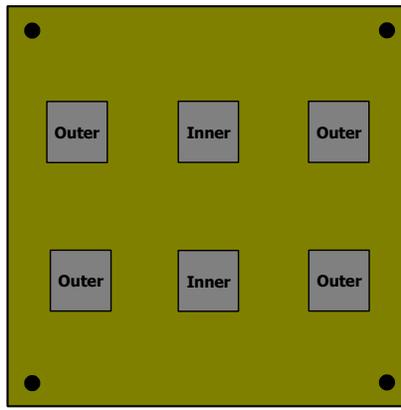


Figure 11. TV2 used in Amkor 12mm Reliability Investigation.

Four different underfill combinations were evaluated, including underfilling the full module, underfilling the bottom package only and finally bonding the top package to the bottom package. Capillary flow was used to underfill the full module and the bottom module only, as shown in Figure 12. Pattern dispensing on the top of the mold cap of the bottom package prior to placement of the top package was the procedure used for bonding the top to the bottom package, as shown in Figure 13.

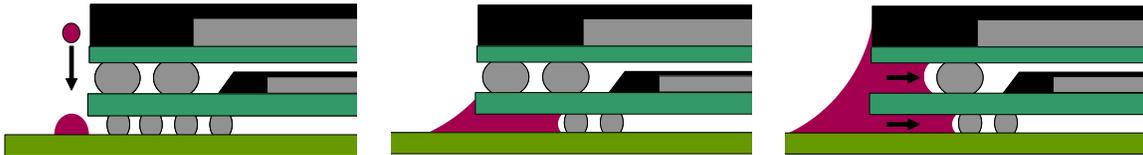


Figure 12. Jet or needle dispensing results in capillary flow. Smaller volumes underfill the bottom only, larger volumes will underfill both levels of the stacked module.

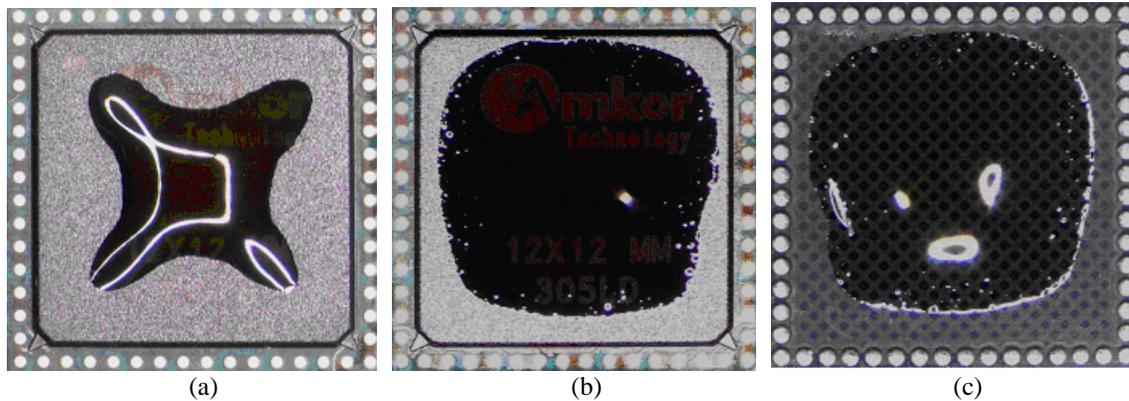


Figure 13. (a) Pattern dispensing on the top mold cap of the bottom package; (b) Underfill coverage after placement of top device; (c) underfill coverage on bottom of top package after placement.

Vibration testing and thermal cycling was performed on this test vehicle. The vibration input was a pure sine wave with a 30-G acceleration amplitude. The driving frequency was set to board resonance (approx. 275Hz) to excite only the first bending mode of the test boards. Failure was determined by manual resistance measurements after every few minutes of testing. In the non-underfilled condition, the top and bottom packages had similar failure rates when located in the outer position. Figure 14 shows the results for all for underfill conditions, both component locations (inner/outer) and top and bottom package cycles to failure. From this graph, the following general observations were made:

1. Non-reinforced components: At the inner location, where board flexure is higher, the bottom component fails first. At the outer location, the top and bottom components fail at about the same number of cycles. This trend agrees with previous drop testing, which showed that the top component becomes more likely to fail first when closer to the supports.
2. Bottom only reinforcement successfully protects the bottom package from failing (no bottom failures were observed in 250k cycles), but transitions the failures to the top location. The overall reliability of the module is lower at the outer location compared to non-underfilled module.

3. Bonding the top package to the bottom package successfully protects the top package from failures (no top failures were observed in 250k cycles). The overall module reliability is comparable to the non-underfilled modules at the outer location, but better at the inner location.
4. Full module underfill successfully protects both levels from failure. No failures were recorded in 325k cycles.

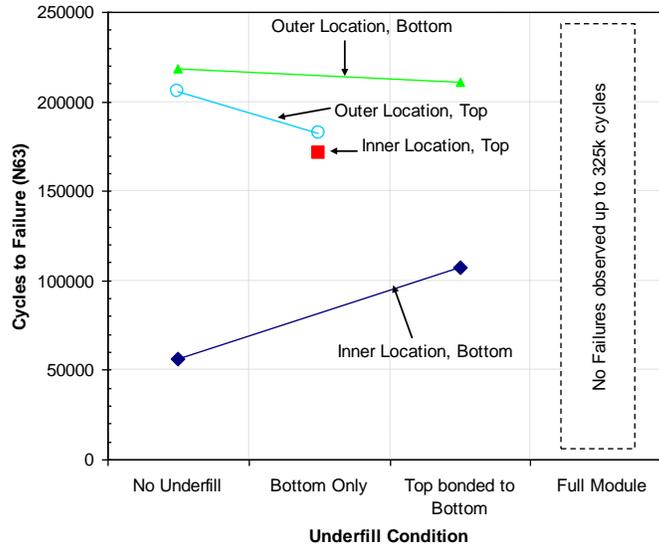


Figure 14. Vibration reliability results for various underfill conditions. Data is split up between inner and out locations, as well as top and bottom package.

Accelerated thermal cycling (ATC) was performed using a -40 °C to 125 °C profile, and 60 minute dwells at each temperature extreme. In this test, both SAC105 and SAC305 balled top components were tested in the full module underfill case. Weibull distributions were fit to the failure data and the characteristic lifetimes are summarized in Figure 15 below. All reinforced cases fail much sooner than the non-underfilled case. The selection of underfill material, and even the top component solder alloy has a large effect on lifetime. Top packages using SAC105 tend to last longer than those using SAC305. The effect of underfill on the mechanical and thermal reliability was similar to other researchers [10].

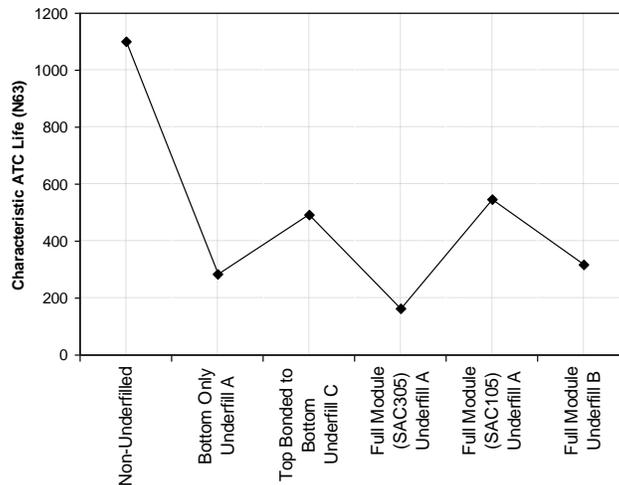


Figure 15. Characteristic Life in ATC for 12mm Amkor PoP.

14mm Package

The 14mm Package from Amkor was evaluated using drop testing. Components were assembled using an in-line process, by flux- or paste-dipping the top component. Dip thicknesses of 30% and 50% were evaluated. Figure 4 shows the top package standoff as a function of dip material and thickness. The test board for this investigation was a live product board which was modified slightly to accept the JEDEC defined board mounting positions [9].

The board dimensions were 150x93mm, 0.8mm thick. Component location effect was considered, with both “inner” and “outer” locations as shown in Figure 16. Loc1, Loc2, Loc3 refer to strain gage placement, as described below.

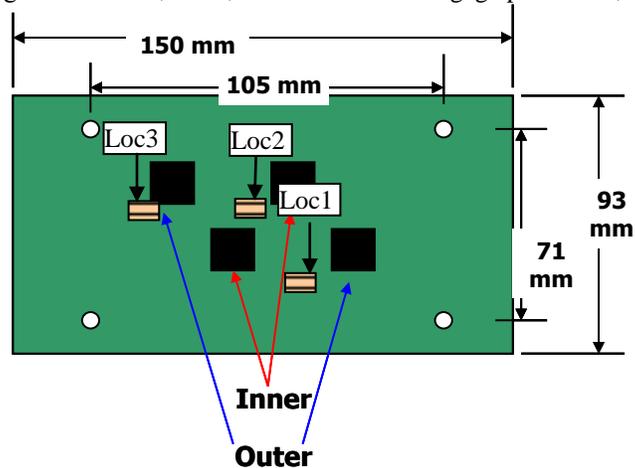


Figure 16. Diagram of Drop Test Vehicle for Amkor 14mm PoP Package.

The previous drop and vibration testing showed that the location of the component on the PCB has a great effect on not only the lifetime, but also the location of first failure (top or bottom package). The dynamic response of this test vehicle was characterized using both the acceleration response as well as strain at various locations on the PCB. Figure 17 shows the acceleration response at the center, inner and outer component locations. Clearly the greatest response is at the center of the board, where the most flexure occurs during the drop event.

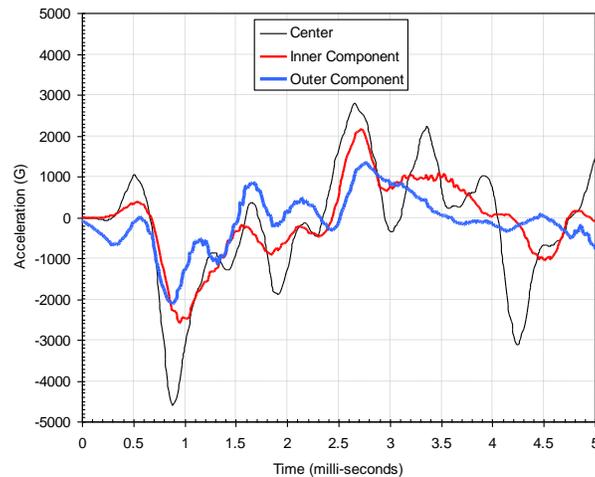


Figure 17. Acceleration response at the board center, inner and outer component locations.

The layout of strain gages, with Loc1 being near a support, Loc2 being near a component corner and Loc3 at the center of the board, are shown in Figure 16. Figure 18 shows the measured strain values during the drop test, in the length, width and diagonal directions. This strain data indicates that the bending along the length of the board is greatest at the center, and reduces closer to the board support. The bending along the width is greatest just away from the center (location 2), and is very small near the supports. Most interesting though, is that the bending along the diagonal of the board is greatest near the supports. All three graphs show a contribution of multiple bending modes, with the first mode being dominant at locations 2 and 3. At location 1, which is near the support, the 2nd mode, which is a twisting mode, is dominant. This particular bending mode may be directly related to transition of failure from the bottom package near the center of the board to the top package near the supports.

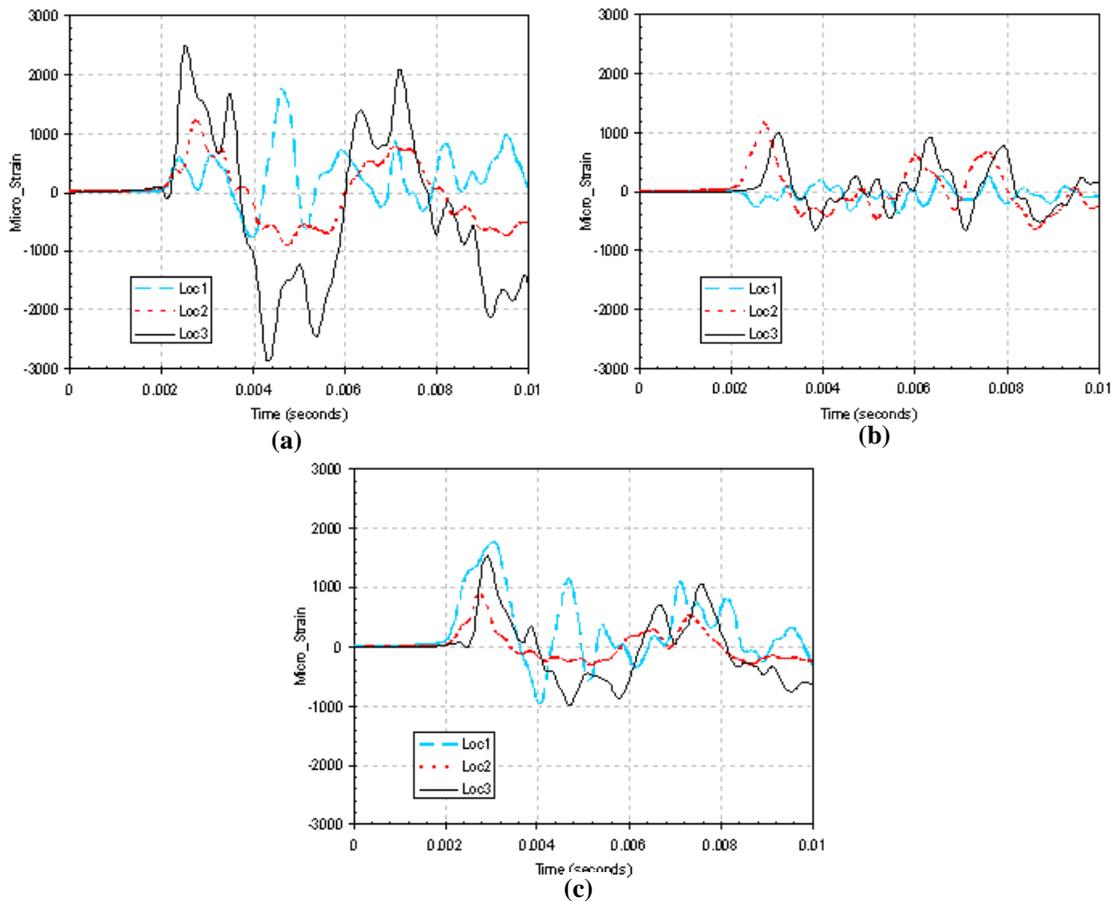


Figure 18. (a) Strain history along horizontal direction; (b) strain history along vertical direction; (c) strain history along diagonal.

Drop testing on these test vehicles was conducted until each particular site had failed, whether by top or bottom package, or until 300 drops, whichever came first. Because of the stipulation that only the full site is required to fail, full failure data for both top and bottom packages is not available. However, the testing indicated that out of 301 tested modules, 294 failed at the bottom package first. There were seven (7) instances where the top package failed before the bottom. Out of those seven (7) top packages that failed first, six (6) were located at the outer component location, which agrees with both previous test vehicles that saw a greater amount of failure of the top package at the outer component location. Figure 19 shows the characteristic lifetime in drop test for the different top package solder conditions. The data reports failure of the module only, whether by top or bottom failure. The data is broken into inner and outer component lifetimes, and shows that the outer components last almost 100% longer than the inner components. The data also shows that paste dipping gives increased lifetime, presumably due to decreased module stiffness from the greater standoff on the top package. This translates into lower stress in both the top and bottom joints during the bending event in the drop.

When the full module is underfilled, only a single failure in 32 tested packages was recorded in 300 drops, which passed the reliability requirements for this particular test vehicle. Again, underfill is shown to be a successful in protecting the stacked module in mechanical loading situations.

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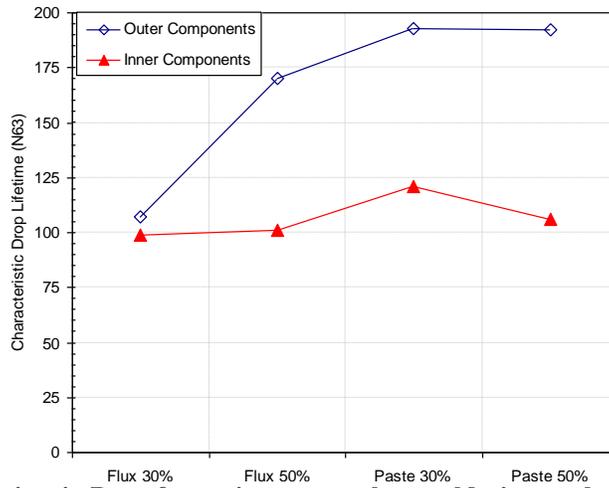


Figure 19. Characteristic Lifetime in Drop for various top package soldering methods, non-underfilled condition.

Bottom package failure modes were either pad cratering of the PCB or intermetallic failure at the component side pad (Cu-Pad). Some PCB pads included a micro-via, and in that case the cratering path included barrel cracking of the copper via. Examples of bottom package failure modes are shown in Figure 20.

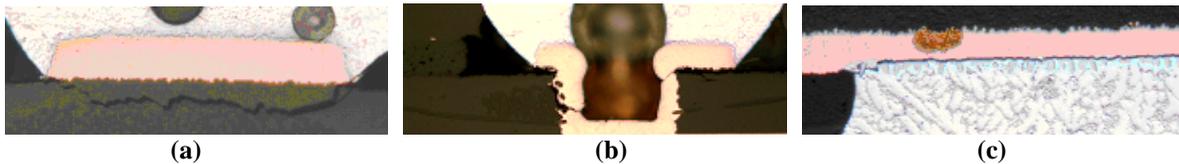


Figure 20. (a) Pad cratering on a surface-pad, (b) Pad cratering causes barrel cracking of micro-via; (c) Intermetallic fracture at the component side (Cu) IMC layer.

This 14mm package was also subjected to ATC, with a thermal profile of -40 °C to 125 °C, with 60 minute dwell times at the temperature extremes. Two PCB surface finishes were used, including CuOSP and ENIG. The top and bottom packages were monitored individually, and it was found that the top package consistently failed before the bottom package. The PCB finish did not affect the top package failure rates, which is expected. However, the PCB finish did affect bottom package failure rates, with the Cu PCB outperforming ENIG by 60%. The failure data is shown by a 2-parameter Weibull distribution in Figure 21.

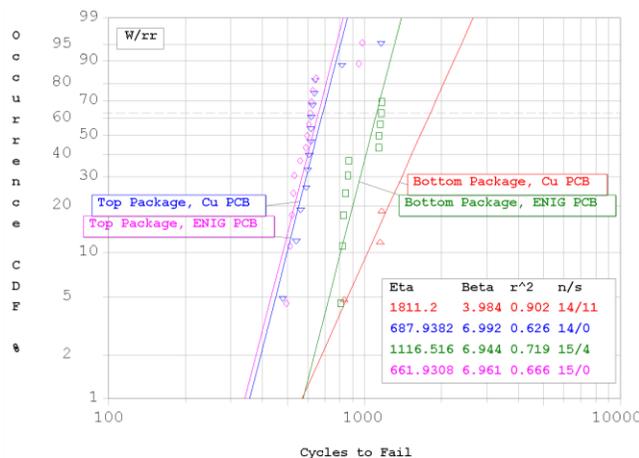


Figure 21. Failure data for ATC on 14mm Amkor PoP, using a Cu and ENIG PCB.

Conclusions

The preceding summarizes several experiments meant to address both the assembly and reliability concerns of Package-on-Package technology. Because the experiments were based on specified test vehicles, direct comparisons between each are not possible. However, general conclusions can be made by observing the trends.

1. In terms of assembly, the warpage of the device during solder solidification is critical. The Amkor 14mm package actually showed more warpage at peak temperature than the devices from Supplier D, but the warpage of the Supplier D package did not relieve until past the solidification temperature. Because of this, head-in-pillow failures were common on the Supplier D package, but not on the Amkor 14mm package.
2. Pre-stacking the packages is a relatively straight forward process, and can be incorporated into existing surface mount assembly equipment. Specialized pallets need to be fabricated for holding the bottom package.
3. In-line stacking is also straight-forward, as long as the placement equipment allows placing one component onto another. Placing the top component is successful using a flux or paste dip, but paste dipping results in a taller joint on the top component. If paste dipping, the proper paste should be selected that has been developed for that process.
4. The drop reliability of the devices is not limited by either the top or bottom package, independently. The trend seen on the various test vehicles presented here shows that the bottom package is most likely to fail when the module is located in an area of high PCB bending. When the module is located closer to a fixed support, the top package becomes more likely to fail. The dynamic board response suggests that the 2nd bending mode (twisting) may be the driving factor for top-package failures. Reliability engineers should take care in generalizing results.
5. Selectively underfilling the top or bottom level individually provides for significant gains in mechanical reliability of that level, but transfers the failure to the other level. The overall module reliability is comparable to non-underfilled devices.
6. Fully underfilling the modules successfully protects the solder joints in mechanical loading, but severely decreases the lifetime in accelerated thermal cycling.
7. The choice of PCB pad finish has no impact on the top package reliability in ATC. However, like other surface mount devices, this will affect the reliability of the bottom package. Our reliability results show that the top package is less reliable in ATC than the bottom package.

Acknowledgements

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References

- [1] L. Smith, M. Dreiza, A. Yoshida, "Package on Package (PoP) Stacking and Board Level Reliability Results", Proceedings of SMTA International Conference 2006, pp.306-312.
- [2] M. Dreiza, L. Smith, G. Dunn, N. Vijayaragavan, J. Werner, "Package on Package (PoP) Stacking and Board Level Reliability, Results of Joint Industry Study", Proceedings of IMAPS 2006.
- [3] A. Yoshida, J. Taniguchi, K. Murata, M. Kada, Y. Yamamoto, Y. Takagi, T. Notomi, A. Fujita, "A Study on Package Stacking Process for Package-on-Package", Proceedings of 56th Electronic Components and Technology Conference, San Diego, CA, May 2006, pp.825-830.
- [4] M. Dreiza, A. Yoshida, K. Ishibashi, T. Maeda, "High Density PoP (Package on Package) and Package Stacking Development", Proceedings of 57th Electronic Components and Technology Conference, Reno, NV, May 2007, pp.1397-1402.
- [5] W. Lin, A. Yoshida, M. Dreiza, T. Yamashita, A. Ishihara, "Control of the Warpage for Package on Package (PoP) Design", Proceedings of SMTA International Conference 2006, pp.320-326.
- [6] JEDEC Standard JESD22-B112, High Temperature Package Warpage Measurement Methodology, May 2005.
- [7] R. Boulanger, "Assembly Challenges of Package-on-Package", Proceedings of SMTA International Conference 2006, pp.338-341.
- [8] P. Wood, "Reworking Package on Package Components", Proceedings of SMTA International Conference 2007, pp.363-367.
- [9] JEDEC Standard JESD22-B111, Board Level Drop Test Method of Components for Handheld Electronic Products, 2003.
- [10] J-Y. Lee, T-K. Hwang, J-Y. Kim, M. Yoo, E-S. Sohn, J-Y. Chung, "Study on the Board Level Reliability Test of Package on Package (PoP) with 2nd Level Underfill", Proceedings of 57th Electronic Components and Technology Conference, Reno, NV, May 2007, pp.1905-1910.