ASEP (APPLICATION SPECIFIC ELECTRONICS PACKAGE) A NEXT GENERATION ELECTRONICS MANUFACTURING TECHNOLOGY

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ABSTRACT

While significant effort and progress has gone into optimizing the transistor density of silicon devices through the use of Application Specific Integrated Circuits (ASIC) that are used in automobiles to watches, limited progress has been made in how electronic sub-assemblies are manufactured. The functioning silicon within devices is still packaged into a Surface Mount Technology (SMT) package, which is placed onto a Printed Circuit Board (PCB), much like the approach used 40 years ago. The demand for smaller, lighter, higher performance, lower cost, and more reliable electronics requires better ways to design and manufacture electronic assemblies.

This paper introduces a novel electronics packaging method known as Application Specific Electronics Package (ASEP). The technology enables the integration of PCBs, connectors, high-current conductors, as well as active and passive components into a single device. ASEP assemblies can have multi-layer circuitry and three-dimensional features. They can be inherently hermetically sealed, manufactured with thermally conductive resins that are effective in dissipating heat, and designed in such a way to benefit from the high conductivity of metal to carry high currents and heat, making the process an ideal solution for assemblies that must withstand high temperatures, high currents, and harsh environments.

In this work, the advantages of ASEP technology, the manufacturing methods, and an example of an application will be discussed. Electrical, thermal and mechanical tests were performed to evaluate the reliability of the package according to automotive requirements. The results have shown that ASEP packages can be successfully used for automotive under the hood electronics. The designed ASEP package is 58% smaller, 22% lighter with 25% improvement in current capacity at 110°C.

Key words: PCBs, ASICs, Power Electronics, Heat Dissipation, High Current Electronics, Inkjet Printing

INTRODUCTION

In 1965, Gordon Moore predicted that the number of transistors that could be packaged into a square inch of space would double every year for the foreseeable future [1]. Although his projection was later revised to every 18 months, “Moore’s Law” has withstood the test of time for five decades. Today, we are beginning to see challenges to this type of exponential growth due to the inherent limits associated with silicon lithography, packaging of the devices, and component placement on PCBs [2, 3]. To provide perspective on the extraordinary rate at which computing power has increased, some estimates conclude that the iPhone 6 released in 2014 could guide 120,000,000 Apollo era spacecraft to the moon all at the same time [4].

One of the methods used to drive this explosive growth in the performance of electronics were ASICs. ASICs allowed designers to package more and more functions into a single piece of silicon. The resulting circuit was not only smaller, but consumed less power, generated less heat, and was significantly less expensive in high volume production [5]. With some scientists predicting that Moore’s Law is no longer valid due to the fact that practical limits are being approached or physics laws would need to be violated, new methods or approaches to designing and manufacturing electronic solutions will need to be developed [2, 6].

While significant effort and progress has gone into optimizing the silicon that goes into everything from automobiles to watches, relatively limited progress has been made in how microprocessors, memory, power devices, passives, sensors, LEDs, etc. are integrated into electronic devices. The functioning silicon within the devices is still packaged into an SMT package which is placed onto a flat PCB, which may or may not have multiple layers much like the approach used 40 years ago [7]. Connectors, support features, heat sinks, and a variety of other electronic components are still discrete devices that need to be soldered, heat staked, welded, glued, through-holed, or assembled in some fashion onto the PCB [8, 9].

The PCBs used to produce nearly all electronics today are manufactured using a subtractive process. Thin Copper (Cu) sheets are glued to the front and back of a fiberglass sheet to manufacture the PCB laminate. Then the assembly is drilled, electroless plated, laminated with a dry film, imaged, developed, electroplated, stripped, etched, solder masked, and removed from a panel to create a finished circuit board [7]. These manufacturing steps are, not only extremely capital- and labor-intensive processes, but also one of the largest users of industrial water. It is estimated that 1500 liters of water are used to manufacture a one square meter PCB (400 gallons per square meter) [10]. The cost of treating the waste water is significant, which results in higher manufacturing costs. Furthermore, at the "end of life" of an electronic product, the conventional PCB assembly is often dumped into a landfill because it cannot be fully recycled.

High current power control and the heat generated by the power devices are becoming a significant challenge in the automotive, commercial vehicle, and industrial equipment industries. Typically, power control electronics have been made with "thick copper" PCBs, where the Cu traces are between 75 and 200 microns thick. These types of PCBs are relatively expensive, and yet they are not very efficient in conducting high current and managing the heat when compared to thicker stamped Cu alloys which may be up to several millimeters thick. Furthermore, if control electronics requiring much finer circuit patterns must be placed on the same PCB, the manufacturing requirements for the signal traces and the power traces conflict.

ASEP attributes allow designers to achieve many of the same advantages at the electronics packaging level that were only possible at the silicon packaging level with ASICs 40 years ago. ASEP manufacturing methods make it possible to integrate the function of multi-layer PCBs, flex circuits, connectors, thermal management features, high current carrying elements, support structures, etc. into a single device which becomes the backbone of the electronics system.

In this work, the advantages of ASEP technology, the manufacturing methods, and the reliability results of an under the hood electronic module manufactured by the ASEP process will be discussed.

Experiment

I) DESIGNING ASEP APPLICATIONS

ASEP not only enables product designers to work more closely together but it also requires them to successfully design applications that will fully benefit from an ASEP based product. This results in a level of collaboration and software compatibility between ECAD, MCAD, FEA, and rendering tools that has not been required in the past. Collaboration between disciplines can only be enabled if either a software package is capable of all of these functions or if it is possible to translate easily and reliably between the software packages. A software package called PCB Connector allows designers to use Altium to complete their multi-layer circuit design [11, 12]. The software translates the Altium data into a parasolids file which can be imported directly into Solidworks or other compatible systems such as NX. The exported electronic layout and components are then used to create the "mechanical features" in the ASEP design and to provide the details for the thermal modeling and industrial design of the product.

Whereas conventional PCBs are made using a subtractive process and require Gerber files that include drill, etched circuit, solder mask, nomenclature, and routing layers [7], ASEP applications are manufactured using additive processing and require a different set of formats. STEP files are used to transfer designs for the manufacture of the stamped metal carriers and for the manufacture of the molds that are used to produce the plastic components. Since all mechanical ASEP features are molded in the second step of the process, no drill, routing, or punching files are required. The formats required for the printing of circuitry onto ASEP substrates are DXF for laser processing, and Bitmap for inkjet printing of conductive ink and solder mask. The benefits associated with having a highly collaborative design process between the various disciplines results in a final product that is smaller, lighter, and more thermally efficient. At the same time, the product will have higher performance and will be cost effective.

II) ASEP MANUFACTURING

New and smarter ways of manufacturing electronics as well as better ways to dissipate the heat being generated must be developed for the electronics industry to continue a robust growth trajectory. An additive manufacturing process, ASEP, builds up the conductive patterns on the surface of the plastic substrate, as opposed to etching the Cu away, and as a result uses less than 150 liters of water per square meter of area. Thermoplastic ASEP substrates can also be re-melted and reused. Figure 1 shows the basic process steps for ASEP manufacturing.

A list of the process steps is as follows:

a) Stamp metal carrier

b) Insert mold plastic substrate

c) Laser modify the surface

d) Inkjet print nanoparticle conductors

e) Sinter to make the traces conductive

f) Electroplate with Cu and additional metals

g) Inkjet print solder mask

h) Dispense or screen solder paste

i) Pick and place components and reflow

j) Singulate

k) Place into final assembly housing

The ASEP process starts with a stamped metal carrier which is over-molded with a high temperature substrate. A nanoparticle ink is used to print the patterns and then the traces are electroplated with conventional metals commonly used in the PCB industry (Fig. 2). A solder mask is applied and then components are reflowed onto the ASEP assembly. This continuous flow process significantly reduces labor, chemical effluent, waste water, and system costs while reducing heat, weight, and the size of the assembly.

The stamped metal carrier within the ASEP assembly serves multiple important functions in the manufacture of the product. The substrate is a way to carry the ASEP assembly through the manufacturing process steps and the electrical contacts for the connector features of the ASEP assembly. In addition, the substrate serves as a method to transfer the heat generated by the components placed onto the ASEP assembly and a path to carry high current that would otherwise be impossible to carry within a conventional PCB assembly. The metal carrier can be formed to be at the surface of the substrate enabling the placement of high power devices directly onto the surface of the metal alloy. Moreover, the substrate acts as a method by which all the electrical traces printed onto the surface of the ASEP assembly can be electroplated using metals that are commonly used in the PCB and connector industry such as Copper, Nickel, Tin, Silver, Palladium, and Gold.

For higher density electronic packages, a two-sided reel to reel manufactured polyimide flexible circuit either replaces or is integrated with the stamped metal carrier, creating up to 5 layers of circuitry. This type of ASEP packaging would be used to design miniaturized consumer electronics, sensors, medical devices, and small wearable devices. Furthermore, the plastic substrate material over molded during the second step shown in Figure 1 can be thermally conductive. If a thermally conductive substrate such as a liquid crystal polymer (LCP) is used, it effectively becomes a heat sink or spreader, reducing the temperatures of the heat generating components [13]. The ASEP process can be highly automated, minimizing the amount of chemical effluent, and dramatically reducing the amount of water required to manufacture electronic assemblies.

After the stamped metal carrier has been over molded with an LCP substrate, a laser is used to define the circuit patterns on the surfaces of the substrate. Since all of the 3D features such a vias, recesses, or ramps have been molded into the substrate, the laser must be able to image the pattern in three dimensions. After the patterns have been laser marked, an inkjet printer deposits a thin conductive layer of metal onto the traces that were defined by the laser. The resolution of the lines and spaces that can be printed using this approach can be as fine as 150 microns. The “seed layer” of conductive traces that was printed onto the substrate is electrically bussed through the vias to the stamped metal carrier. This provides the electrical connections which enable the entire ASEP module to be electroplated. The remaining process steps are common to the PCB assembly market.

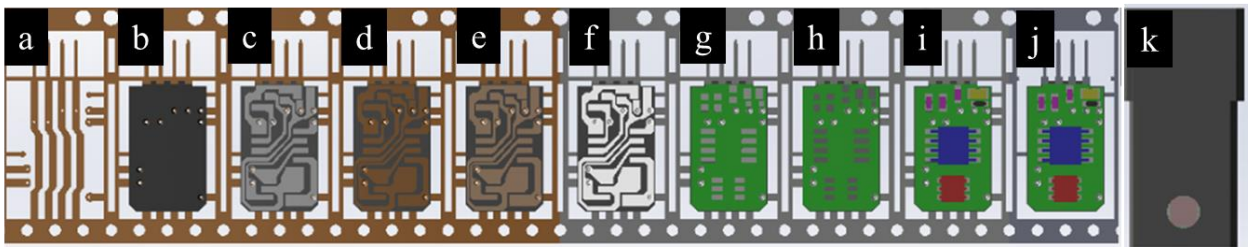

Figure 1: ASEP manufacturing process from stamping to reflow. The process is continuous and requires roughly half as many process steps as conventional PCB manufacturing.

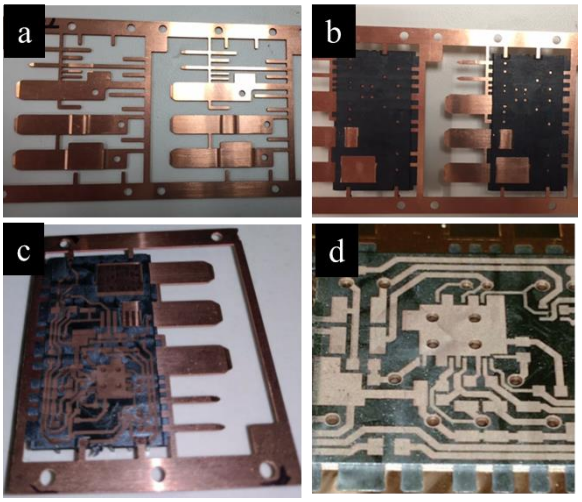

Figure 2: Four steps of ASEP manufacturing: a) metal stamping b) over molding with LCP c) laser marking the surface d) inkjet printing of nanoparticle metal.

III) ASEP ATTRIBUTES AND FEATURES

Like an ASIC which combines the functionality of multiple silicon devices into one smaller device that consumes less power, reduces heat, is less expensive, and has more functionality, an ASEP design is unique in that it enables designers to develop applications that are often smaller, more thermally efficient, with higher performance, and result in a lower system cost. While ASICs achieve these results at the silicon level, ASEP achieves these results at the electronic component and PCB level.

By integrating the functionality of a PCB, connector, and thermal management features, ASEP combines the functions into a single device which will be smaller, lighter, and more efficient. Because the process is fully additive, 90% less water is consumed where compared to PCB manufacturing and there is virtually no chemical effluent in the manufacturing process. The ASEP process reduces the capital requirement as well as the labor content since it is a highly automated process. Several additional advantages are that ASEP applications can be made to be inherently hermetically sealed. The combination of these advantages should result in very cost effective electronic solutions.

Figure 3 shows an ASEP package without components. The package, called ASEP MicroPDB (Micro power distribution box), adds additional power switching and circuit protection to the vehicle's wiring architecture. The two high current electrical paths for the Field Effect Transistor (FET) in the lower bottom corner of the device are extensions of the actual metal contacts. Therefore, the FET as is shown in Figure 4 is soldered directly to the 800 micron thick Cu alloy, the resulting electrical and thermal path has been optimized. This reduces the resistance in the system (reduces heat generated) and reduces the resistance in the thermal path to remove the heat from the device very efficiently. Furthermore, the ASEP material used for the application can be a thermally conductive plastic (such as LCP) which spreads the heat generated by the FET. In effect, the ASEP material itself can be the heat sink or spreader, making it possible to reduce the temperature of the heat generating devices.

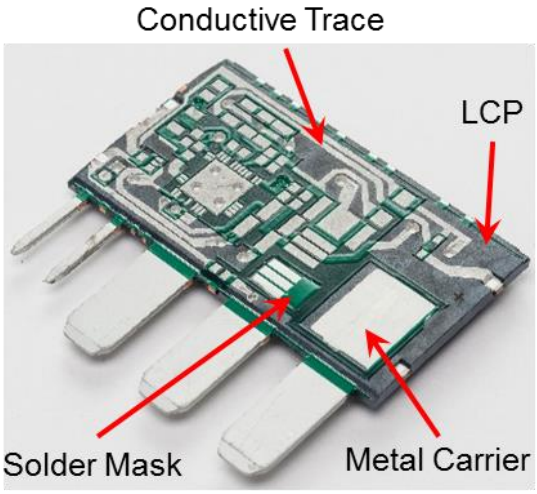

Figure 3: An ASEP MicroPDB substrate without components. The FET will be soldered to two of the contacts on the MicroPDB that are direct extensions of the 800 micron thick Cu alloy contacts (cf. Fig. 4).

The ASEP MicroPDB is a power control device that looks very much like an automotive connector (see Figure 4) but within it a microprocessor and FET provide Local Interconnect Network (LIN) control and high current solid state switching that are highly reliable, self-protecting, and cost effective in comparison with a current MicroPDB containing a relay and fuses (cf. Fig. 5). The microprocessor provides LIN control which eliminates the need to run control lines to each device.

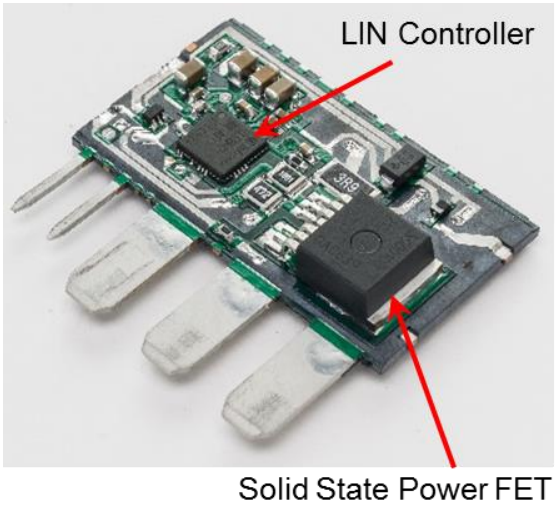

Figure 4: The FET is soldered directly to the thick Cu alloy contacts. This results in low thermal and electrical resistance between the heat generating FET and ambient.

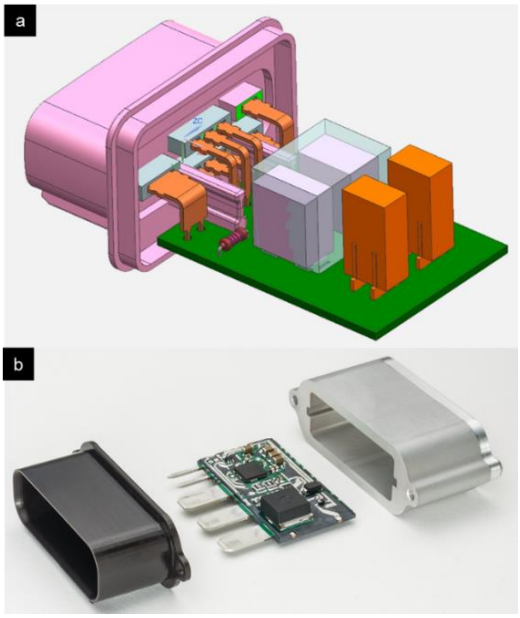

Figure 5: Image a) current PCB based MicroPDB with relay and fuses b) an ASEP MicroPDB with FETS.

IV) ELECTRICAL, THERMAL and MECHANICAL TESTING

The ASEP MicroPDB was the application used for validating the use of the technology for under the hood power electronics. The verification that a new manufacturing technology will meet all the requirements for a specific industry is an important first step in ensuring that the end product will satisfy the stringent requirements of the automotive electronics market. The ASEP MicroPDB was evaluated using a customer's engineering specifications. Tests performed, such as thermal shock and vibration, are intended to simulate an accelerated life test for power electronics.

Three main tests were performed to evaluate the electrical, thermal and mechanical performance of the ASEP MicroPDB. First, temperature rise testing was performed on the package. The ASEP microPDB was powered with 12 V from 0 Amps to shut down in 5A intervals and 30 minute intervals. Thermocouples were attached to the microprocessor and the FET to measure the temperatures. Tests were conducted at both 85°C and 110°C ambient. According to specification, the temperature rise should not exceed 55°C above the ambient temperature. In addition to the temperature rise test, both thermal shock and vibration tests were performed according to USCAR 2 revision 6 specification [14]. After the test, the voltage drop was measured and a continuity test through each circuit was performed. Samples were visually inspected to determine any visible cracks or distortions.

RESULTS

Figures 6 and 7 show some of the data collected during the temperature rise testing of the ASEP MicroPDB.

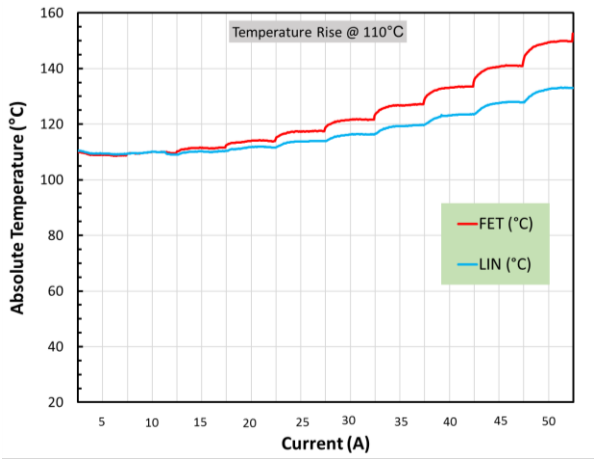

Figure 6: Temperature rise vs. current at 110°C ambient for the ASEP MicroPDB

The data shown in Figure 6 was taken at 110°C ambient and provides the basis for the rating of the current carrying capacity for the device. The data provided in Figure 6 shows the temperatures at the FET and microprocessor over time and input current during power dissipation testing. The red curve in Fig. 6 shows the temperature of the FET case temperature. The results confirm that the ASEP microPDB is capable of carrying 50 Amps of current at 110°C ambient. The package shuts down at higher currents as the temperature rises more than 55°C above ambient.

Figure 7 shows the overload test performed on the ASEP package. To ensure that the system protects itself during overload conditions, the current is increased to 140% of its rated power (i.e. 50 Amps). The part is functional after the overload test.

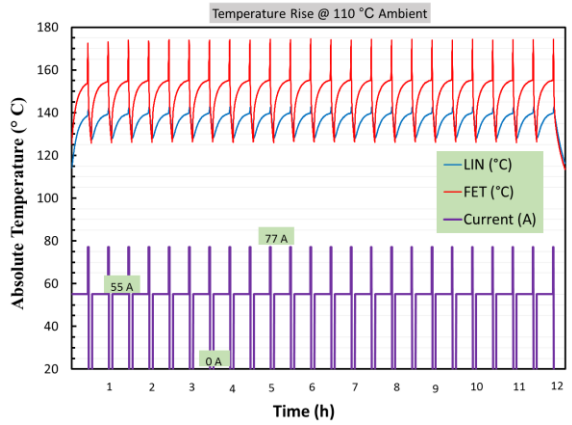

Figure 7: Temperature rise vs. current data at 110°C ambient during power dissipation testing of the ASEP MicroPDB.

With ASEP, the stamped metal features used to carry the very high current and spread the heat can be exposed on either the upper or lower surface of the ASEP assembly. This makes it possible for the heat generating devices to be soldered directly to the thick Cu Alloy stamping, thus

enabling the heat to be dissipated much more efficiently. The ASEP MicroPDB that was evaluated is rated to carry 50 Amps at 110°C ambient (Fig. 6). In addition to a thermal test, the ASEP assembly met all the requirements of the vibration and thermal shock tests.

Table 1 provides a comparison between the size and weight of a PCB MicroPDB design currently in production and the ASEP MicroPDB design. The ASEP MicroPDB is 58% smaller and 22% lighter with an improved current capability at higher temperatures.

It is well known that the mismatch in the coefficient of thermal expansion (CTE) between substrate and component is the main reason for the failure of solder joints and thus electronic packages [14]. Due to lower CTE mismatch between the component and the substrates in the ASEP packages, it is expected that the ASEP package will show superior reliability performance compared to PCB based packages.

Table 1: Comparison of the PCB MicroPDB and the ASEP MicroPDB design.

Feature	Micro PDB	ASEP MicroPDB	Delta
Size	122.5 cm^3	51.5 cm^3	58% smaller
Weight	64 grams	50 grams	22% lighter
Current Capability @ 110°C	40 Amps	50 Amps	25% higher

FUTURE OPPORTUNITIES

Bare Die Packaging

Bare Die is currently packaged into component level devices, which are called first level packages [5, 16], and then soldered onto PCBs, which are called Second Level packages. This approach to packaging electronics has basically remained the same for decades, with the primary improvements being in the density of the packaging, the number and type of connections in the first level device, and the methods of interconnection. Whenever a silicon die needs to be packaged into a component before it can be placed onto the PCB, its size increases significantly (often by an order of magnitude) and cost can double. The integration of bare die directly into ASEP devices could dramatically reduce the size, increase performance, and reduce the cost of next generation electronics (Fig. 8).

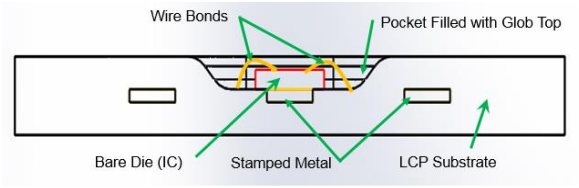

Figure 8: A cross sectional view of a bare die packaged into an ASEP substrate.

Figure 8 shows how a pocket will be molded into the ASEP device and the wire bond interconnects will be plated into the bottom of the pocket. After the die is attached to the substrate, the wire bonds will be completed, and then a glob top will be used to fill the pocket.

CONCLUSION

ASEP is a design and manufacturing process that allows us to take advantage of the benefits of highly conductive metal alloys to remove heat, to carry high current, and to provide reliable electrical interconnects. The technology also enables designers to take full advantage of the properties of high performance injection moldable plastics to create products that can be highly automated with significantly fewer process steps and greater functionality, use dramatically fewer natural resources, and be cost effective. One of the markets that will benefit from the first ASEP applications is the transportation industry due to the rapid growth in the electrification of vehicles along with the exponential increase in the amount of entertainment, safety, sensing, and communication features. Other markets that will benefit from the use of ASEP include consumer electronics, sensor packaging, medical devices, wearables, military, and aerospace systems.

In this work, the advantages of ASEP technology, the manufacturing methods, and an example of an application were discussed. Electrical, thermal and mechanical tests were performed to evaluate the reliability of the package according to automotive requirements. The results have shown that ASEP packages can be successfully used for automotive under the hood electronics. The designed ASEP package is 58% smaller, 22% lighter with 25% improvement in current capacity at 110°C.

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