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Approaches to Overcome Nodules and Scratches on Wire Bondable Plating on PCBs

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Abstract
Initially adopted internal specifications for acceptance of printed circuit boards (PCBs) used for wire bonding was that there were no nodules or scratches allowed on the wire bond pads when inspected under 20X magnification. The nodules and scratches were not defined by measurable dimensions and were considered to be unacceptable if there was any sign of a visual blemish on wire bondable features. Analysis of the yield at a PCB manufacturer monitored monthly for over two years indicated that the target yield could not be achieved, and the main reasons for yield loss was due to nodules and scratches on the wire bonding pads.

The PCB manufacturer attempted to eliminate nodules and scratches. First, a light scrubbing step was added after electroless copper plating to remove any co-deposited fine particles that acted as a seed for nodules at the time of copper plating. Then the electrolytic copper plating tank was emptied, fully cleaned, and filtered to eliminate the possibility of co-deposited particles in the electroplating process. Both actions greatly reduced the density of the nodules but did not fully eliminate them. Even though there was only one nodule on any wire bonding pad, the board was still considered a reject. In order to reduce scratches on wire bonding pads, the PCB manufacturer utilized foam trays after routing the boards so that they did not make direct contact with other boards. This action significantly reduced the scratches on wire bonding pads, even though some isolated scratches still appeared from time to time, which caused the boards to be rejected. Even with these significant improvements, the target yield remained unachievable.

Another approach was then taken to consider if wire bonding could be successfully performed over nodules and scratches, and if there was a dimensional threshold where wire bonding could be successful. A gold ball bonding process called either stand-off-stitch bonding (SSB) or ball-stitch-on-ball bonding (BSOB) was used to find out the effects of nodules and scratches on wire bonds. The dimension of nodules including height, and the size of scratches including width were measured prior to wire bonding. Wire bonding was then performed directly on various sizes of nodules and scratches on the bonding pad, and the evaluation of wire bonds were conducted using wire pull tests before and after reliability test. Based on the results of the wire bonding evaluation, the internal specification for nodules and scratches for wire bondable PCBs was modified to allow nodules and scratches with a certain height and a width limitation, compared to initially adopted internal specifications of no nodules and no scratches. Such an approach resulted in improved yield at the PCB manufacturer.

Introduction
The development of chip-on-board (COB) type of image sensors has significantly increased in the last few years to accommodate an increasing demand for low cost and high-performance industrial inspection cameras. Wire bonding is the most commonly used technology for making the electrical interconnection between a silicon image sensor and its substrate during image sensor fabrication. Therefore, wire bonding directly on the PCB surface is inevitable for COB type image sensor fabrication.

IPC-A-600J[1] lists in section 2.7.1.3 Surface Plating – Wire Bond Pads that "Wire bond pads are free of surface nodules, roughness, electrical test witness marks or scratches that exceed 0.8um (32uin) RMS (root-mean-square) in the pristine area in accordance with an applicable test method AABUS." Since the tolerance of surface nodules, <0.8um RMS, in IPC-A-600J for wire bonding pads is not easily measurable and may not properly reflect single nodules and shallow scratches, the initially adopted specification for wire bonding pads as a user was defined to be free of surface nodules and scratches. Therefore, a board was considered a reject if a nodule or a scratch was visible in the pristine area of the wire bonding pad at 20X magnification. If in any doubt, one could use 40X magnification for inspection to clarify pass/fail. However, in reality, it was difficult to achieve a wire bonding surface in specification without nodules or scratches, resulting in low yield at the PCB manufacturer. Particularly, PCB products designed with a center cut-out slot close to bonding pads were prone to significant yield loss due to nodules.

Yield review with the manufacturer and the analysis of causes for rejects using Pareto Charts pointed out that two main reasons for PCB rejects were actually due to nodules and scratches on the wire bonding surface. Yield had been reviewed on a monthly basis for 28 months, and the major yield losses continued to be due to nodules and scratches on the wire bonding surface during the period. Figure 1 shows the average yield loss per month for wire bonding boards due to nodules and

scratches. The average yield loss from multiple PCB products due to nodules and scratches for wire bonding boards were in the range of 4% to 41% and 2% to 30%, respectively, during the period.

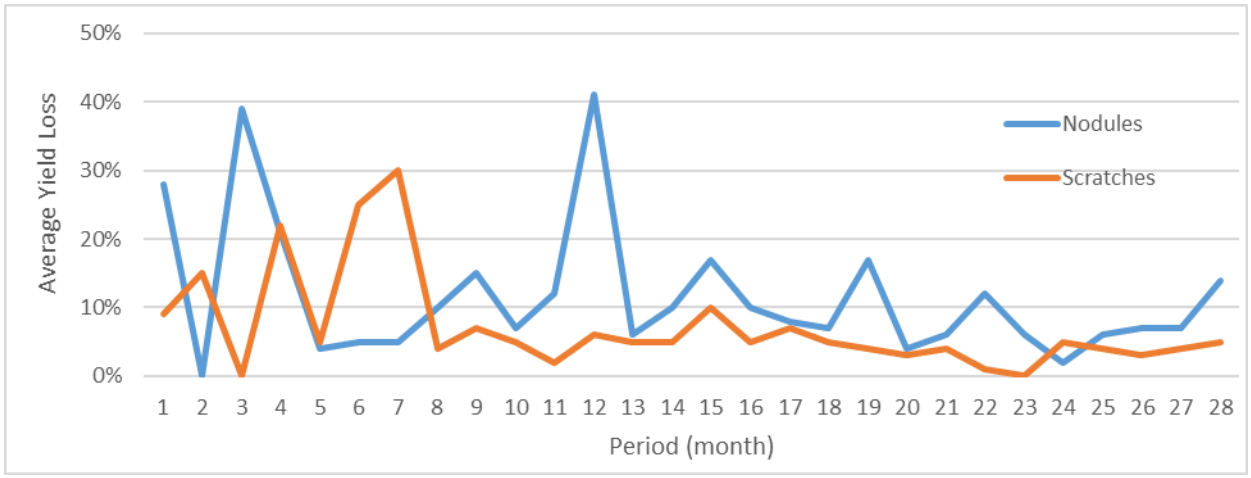


Figure 1 - Average Yield Loss from Multiple Wire Bonding PCB Products

It is worth to note that the data in Figure 1 may not necessarily provide the picture of actual average yield loss due to nodules and scratches. When any defect, either nodule or scratch, was first found during inspection of a board, the reason for reject was recorded, and further inspection of that board was not pursued since the board was already determined as a reject. For example, the manufacturer recorded 39% of yield loss for nodules, and none for scratches in the period 3. However, it may not mean that there were no scratches on those rejected boards since those boards had not been inspected further for scratches after nodules were first observed.

Figure 2 shows the maximum yield loss for nodules and scratches. The maximum yield loss was recorded from one of the PCB products that showed the lowest yield at the period or in the month. Unacceptable yield loss over the period of many months initiated a discussion with the manufacturer in order to identify the root cause and conduct corrective actions to improve on nodules and scratches.

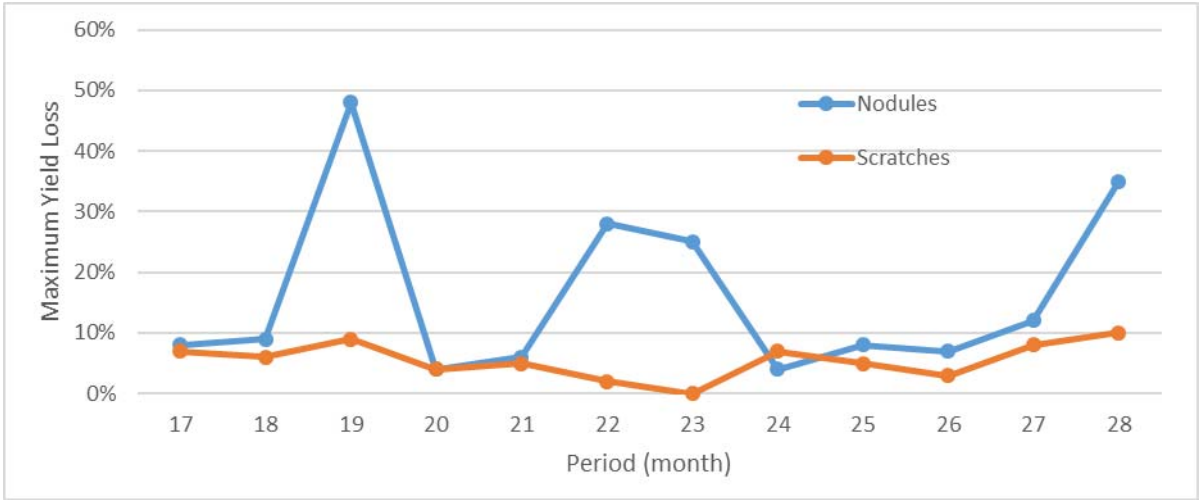


Figure 2 – Maximum Yield Loss from a PCB Product with the Lowest Yield

Corrective Actions at the Manufacturer

The PCB Manufacturing Process

One of the PCB manufacturers who had experience producing the bare boards had considerable data that suggested that nodules and scratches were likely the main reasons for yield loss. The specification initially defined by the user required

inspection at 20X starting magnification, which was beyond the IPC specification of 1.75X magnification. Since there were inspection escapes, the manufacturer decided to start at 40X magnification as a preventative measure. This, combined with the criteria for absolutely no nodules or any surface imperfection, resulted in many rejected boards, which may have actually been wire bondable and reliable. The manufacturer initiated root cause analysis to determine the source of the nodules and scratches in order to define an action plan to reduce or eliminate the defects.

Nodules

Nodules are surface imperfections on the plated surface which can originate and grow in the copper plating process or originate from processes preceding copper plating and grow in the copper plating process (i.e. electroless copper). Electroless copper plating is used as a metallization process that deposits a thin layer of copper onto non-conductive surfaces, such as the hole wall of a drilled panel. This creates electrical connectivity through the plated holes. Then, electrolytic copper plating process uses an electrical current to electrodeposit copper from a copper sulfate solution onto the copper clad production panel. Electroplating inherently prefers to plate onto protruding features, edges, or corners; therefore the slightest surface protrusion on the base copper foil or a minor imperfection co-deposited during the electroless copper process will attract more copper plating and grow in size to become a visually detectable nodule after electroplating.

Nodules that were observed optically under 40X magnification were cross sectioned in an attempt to determine the process at which the nodule began to form. Given the small size of the nodules and knowing that the nodule starts with an even smaller surface imperfection that grows through electroplating, cross sectioning down to the absolute center of the nodule was difficult to achieve and objective evidence of the nodule's origin could not be found all the time. Figure 3 shows an example of a nodule cross-sectioned. In this case, it seemed to be clear that the nodule was formed prior to the Ni/Pd/Au plating process, and, therefore, nodule formation would have likely happened during electroless or electrolytic copper plating.

Figure 3 – Cross-sectioned View of a Nodule as an Example

Using a fishbone diagram to define potential root causes of the nodules, a short list of potential root causes was identified: copper foil imperfections, electroless copper co-deposited particles, and electroplated copper co-deposited particles. Each potential root cause was explored in-depth to prove or disprove that it was the source of – or contributed to – the formation of nodules.

A random sample of copper foil was visually inspected under 100X magnification and no significant signs of imperfections were found. Using a controlled production lot, a light mechanical scrubbing process was performed on the laminated foil through a horizontal conveyorized machine, but the number of boards that were rejected for nodules remained close to the average from previous production lots. Consequently, this potential root cause was eliminated early into the investigation. The same mechanical scrubbing process was performed on panels that had been processed through electroless copper. In this case, the results were noticeable. The density of nodule occurrences was reduced but there were still boards being rejected for single nodules located at wire bond locations. And in some production lots, the frequency of the single nodules was excessive enough to still have a significant impact on yield. However, an overall improvement had been made and this mechanical scrubbing process became a standard process.

After an extended period of processing boards with the mechanical scrubbing process after electroless copper, an opportunity to test the electrolytic copper plating process arose when an annual preventative maintenance procedure was completed on one of the three plating tanks on the automated plating line. The procedure involves: a complete carbon treatment of the copper sulfate-based chemistry to remove organic molecules that have leached out from the dry film photo resist, emptying and cleaning all copper anode baskets to remove copper sludge, replacement of all anode bags, and dummy plating after chemical additions to form a uniform copper oxide film over the anodes. Panels were plated in the new tank and a normal tank, and the amount of nodules were significantly reduced on the panels plated in the new tank. This test was repeated a couple of more times with the same results. As an interim action, all wire bond technology boards were plated in the new tank and this limited the amount of nodules to a consistent value for each lot. Subsequently, the remaining two plating tanks underwent the annual preventative maintenance procedure and all tanks were able to plate wire bond boards consistently.

Although the process improvements significantly reduced the amount of nodules and made the process more consistent, a percentage of boards were still being rejected at Final Inspection for small nodules. It was important to understand the impact that these small nodules have on wire bonding; particularly which size does a nodule begin to negatively impact the wire bonding process.

Scratches

Scratches refer to a surface imperfection with any depth or a discernible non-uniform contrasting marking. Scratches can originate over the base copper, over the plated copper, or over the final finish plating.

When scratches are over the base copper, the plated copper is capable of filling up minor scratches to a certain degree, but significant depths will have plated copper conforming to the surface topography. Likewise, the final finish – which in this case is typically ENIG or ENEPIG – also conforms to the surface topography. Although there is a depth at the scratch, the conductive feature is fully plated with a solderable and wire bondable surface finish. This is the same situation when scratches are over the plated copper.

When scratches are over the final finish, the results can vary depending on the magnitude of the scratch. Deep scratches could potentially break through the final finish and expose copper, which would oxidize and would not be solderable or wire bondable at that location. Surface scratches could expose the nickel which would also oxidize rapidly and cause solderability and wire bonding challenges. Light scratches that only abrade the gold, but does not remove the gold entirely, would still function as a normal solderable and wire bondable feature.

In general, it was found that the majority of boards being rejected for scratches were being scratched after the final finish had been applied. An audit of the process flow of the panels after final finish was conducted and the audit discovered that the scratches were occurring after depanelization of the boards in the routing process. After routing, the boards are washed off and stacked in trays in preparation for electrical testing. Boards were making direct contact with each other resulting in light scratches and surface scratches.

A corrective action was taken to produce foam trays with slots for individual boards so that the boards do not make contact with each other after depanelization. After the corrective action was implemented, the amount of scratches on the boards was significantly reduced but there was still a small quantity of boards being rejected for minor scratches. As was the case with nodules, it was apparent that scratches needed to be characterized to determine their effect on the wire bonding process.

Internal Corrective Actions

Wire bonding on nodules and scratches

Despite significantly reducing the occurrences of nodules and scratches, they were not completely eliminated. Even if there was only one small nodule or scratch on any wire bonding pad, the board was still considered a reject, and therefore, the target yield remained unachievable. This was the reason for further investigation on the effect of nodules and scratches on the wire bonding process.

The type of plating applied to PCBs used for this study was Electroless Nickel/Electroless Palladium/Immersion Gold (ENEPIG) with plating thickness specifications as follows; 3.0-6.0um Ni, 0.15-0.3um Pd, and 0.03-0.06um Au. PCBs rejected due to nodules and scratches were received from the PCB manufacturer. Nodules and scratches on rejected PCBs were inspected under a high magnification optical microscope with image analysis software that was capable of creating 3D images and profiles. The height of the nodules was measured on 3D profile images. PCBs rejected due to nodules were from two different PCB products (i.e., two different PCB designs with different part numbers, called Product I and Product II hereafter) while PCBs rejected due to scratches were only from one of products, Product I. Product I had three different

types of nodules that might be formed by different mechanisms or at different PCB manufacturing process steps based on the appearance of the nodules while Product II had only one type of nodule. Nodules observed from Product I and Product II were arbitrarily divided into three types based on the appearance in this study, and designated as Type A, B, and C. In this study, the effect of nodules on the wire bonding process was only focused on isolated nodules or small nodules formed along a small mechanical defect, so that a wire bond was only interrupted by a single nodule, rather than by multiple nodules. The PCB samples rejected by the manufacturer due to nodules and scratches are summarized in Table 1.

Table 1- PCBs Rejected due to Nodules and Scratches

PCB Product	Plating Type	Nodules	Scratches
Product I	ENEPIG	Nodules with type A, B, and C	Shallow scratches
Product II	ENEPIG	Nodules with type A only	No scratches

The three different types of nodules observed from Product I are shown in Figures 4, 5, and 6. Type A nodules as shown in Figure 4 were most commonly observed. Type A nodules are relatively circular in shape when it is viewed from the top, and has a grain structure on the nodule surface. The cross-sectioned view in Figure 3 appears to be this type of nodule. The diameter of nodules is mostly in the range of 30-50um. The 3D optical microscope image is on the left, and the matching 3D profile view with nodule height is on the right of the figure. Type B nodules as shown in Figure 5 are not circular (or not symmetrical) in shape, and the surface of the nodule looks very smooth without any grain structure. Type C nodules as shown in Figure 6 are formed along any mechanical defect such as a nick. Any protrusions on the surface in the plating steps seems to turn into a nodule. An example of a Type A nodule observed from Product II is shown in Figure 7. Type A nodules were observed only from Product II.

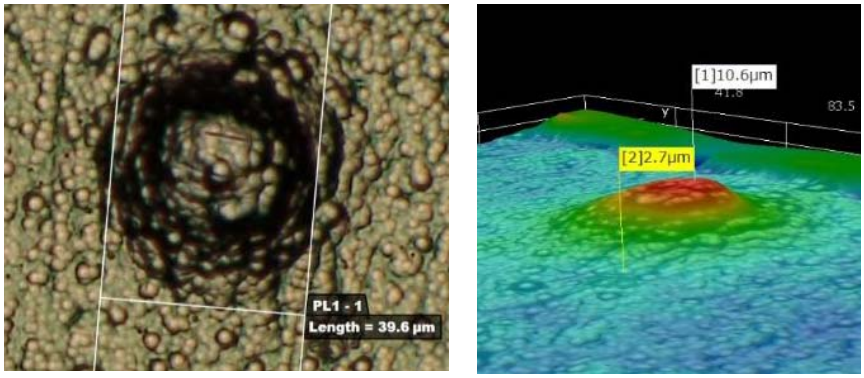


Figure 4 – Example of Type A Nodule Observed from Product I

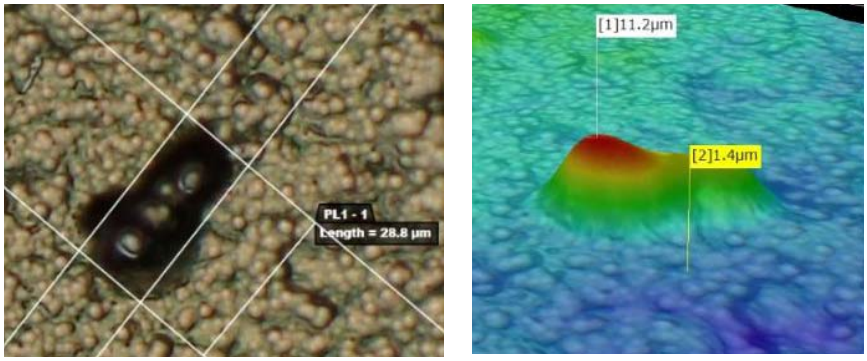


Figure 5 – Example of Type B Nodule Observed from Product I

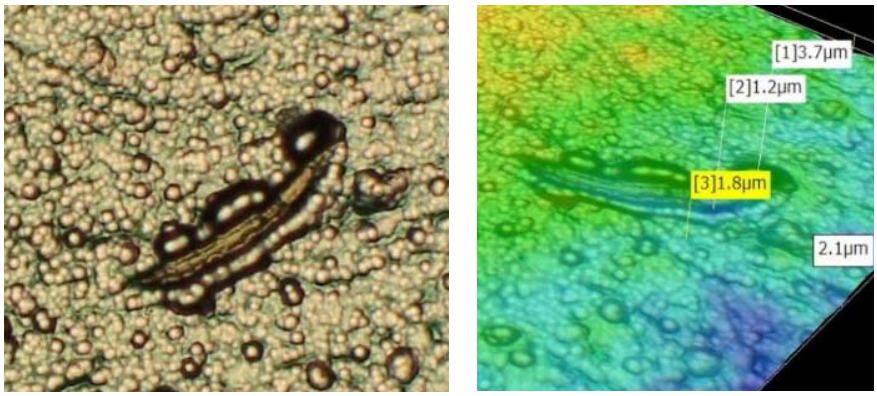


Figure 6 – Example of Type C Nodule Observed from Product I

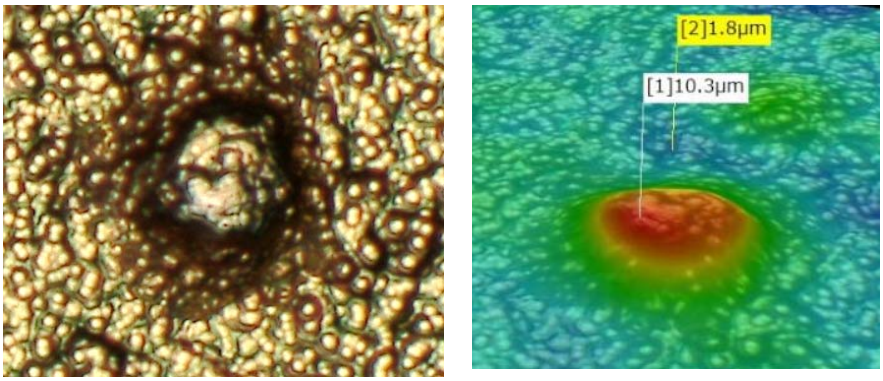


Figure 7 – Example of Type A Nodule Observed from Product II

Figure 8 and Figure 9 show examples of scratches on the wire bonding surface on rejected PCBs of Product I from the manufacturer. Those scratches seem to be made after the final surface finish step since the gold layer looks damaged due to the scratch. The widths of the scratches were about 9um and 20um as shown in Figures 8 and 9.

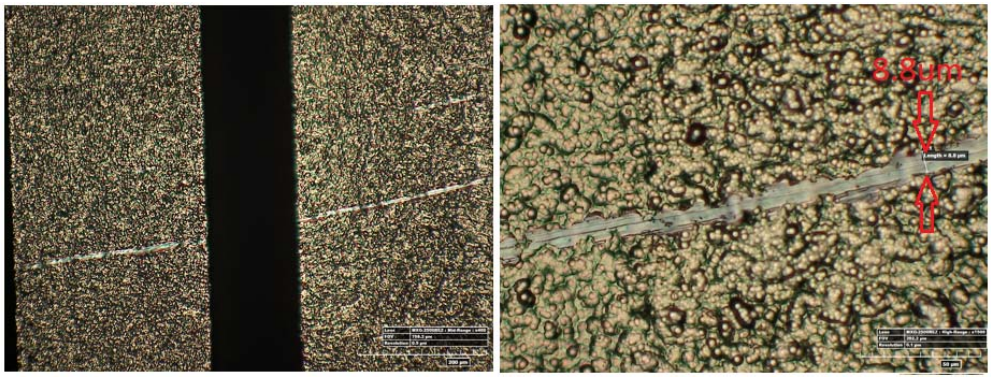


Figure 8 – Scratches Observed on Wire Bonding Track on Rejected PCBs at Low Magnification on the Left and High Magnification on the Right

Figure 9 – Scratch Observed on Individually Defined Wire Bonding Pad on Rejected PCB

The wire bonding process used in this study is a specialized gold ball bonding process called either stand-off-stitch bonding (SSB) or ball-stitch-on-ball (BSOB) in the industry. The diameter of bonding wire used was 25um. Figures 10 and 11 show an example of the SSB process in which ball bonds (or bump bonds) are made on PCB bonding pads as well as on the die bonding pads unlike the standard gold ball bonding process as shown in Figures 12 and 13[2]. For the standard gold ball bonding process, ball bonds are expected on die bonding pads, and stitch bonds are expected on PCB bonding pads. For the standard gold ball bonding process, the wire bonding tool is directly in contact with PCB bonding pads during stitch bonding process. One can see the circular tool mark on the bonding pad in Figure 13. For the SSB process, the bonding tool is not directly in contact with PCB bonding pads, but sits on top of ball bonds on PCB bonding pads.

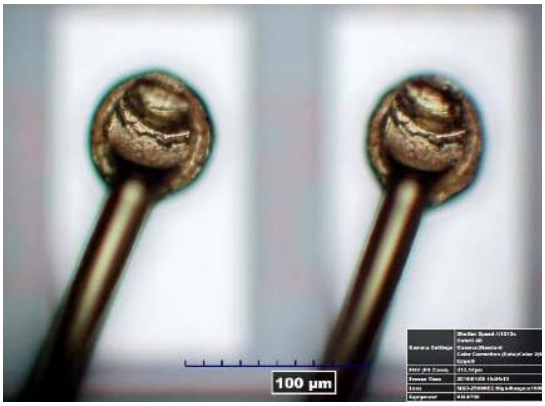


Figure 10 Bonds on Die for SSB Process

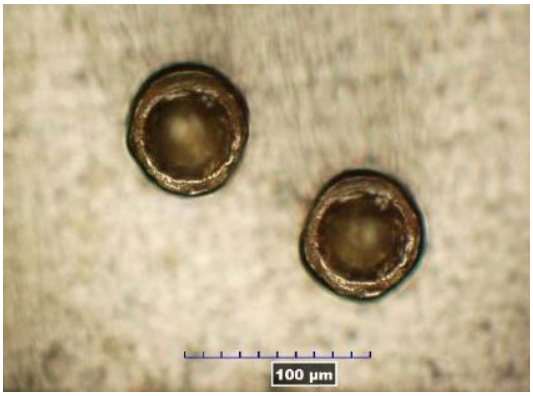


Figure 11 Bonds on PCB for SSB Process

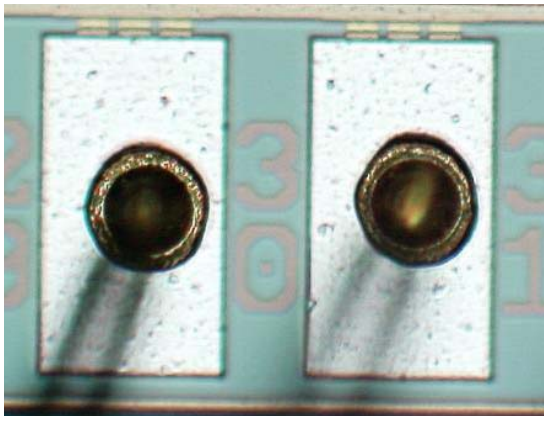


Figure 12 Bonds on Die for Standard Ball Bonding Process

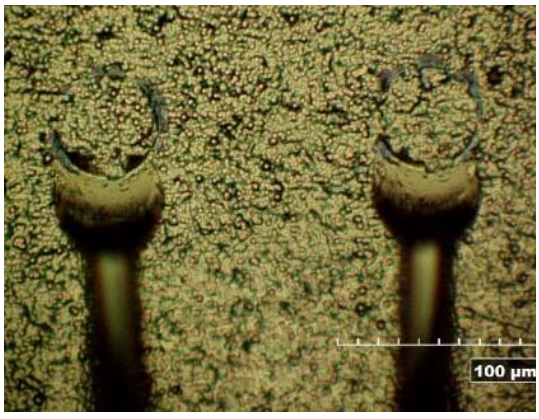


Figure 13 Bonds on PCB for Standard Ball Bonding Process

The height (or thickness) and the diameter of ball bonds made using the SSB process on PCB bonding pads are around 13um and 63um for Product I, and 15um and 62um for Product II. The dimension of ball bonds on PCB bonding pads would be considered a critical factor for a wire bonding experiment on nodules and scratches. The height of ball bonds directly indicates the height of the bonding tool from the bonding pad at the time of wire bonding since the bonding tool sits on the ball bond. In theory, ball bonds might not be squashed as much as programmed if the wire bonding tool touches a tall nodule before the ball bond is squashed as much as programmed. Therefore, it is likely that the acceptable nodule height might be related to the height of the bonding tool from the bonding surface at the time of wire bonding. In addition, ball bonding on an uneven surface due to nodules would be a factor for the integrity of wire bonds, and the height (or thickness) of ball bonds would be the amount of buffer that can conform with the shape of the nodules. In this aspect, the SSB process compared to the standard ball bonding process would be much more beneficial on wire bonding on nodules. The diameter of ball bonds is also directly related to the wire bond contact area on PCB bonding pads. Therefore, when wire bonds are made on surface imperfections such as nodules and scratches, the percentage of wire bond area made intact on the bonding pad without any surface imperfections is determined by the ball bond diameter (i.e., area).

The integrity of wire bonds was measured by wire pull tests before and after reliability testing. Wire bonds were made directly on nodules and scratches even though the alignment of wire bonds on nodules and scratches varied slightly, so that, some bonds were aligned slightly better than the others. There were only a couple of PCBs rejected by the manufacturer due to scratches, and therefore, there were not enough scratches with varying widths to make wire bonds in order to determine the maximum allowable scratch width. For this reason, scratches with various widths were artificially created on PCB bonding pads by using a sharp knife blade for PCB Product I. However, the depth of artificially created scratches as well as that of scratches on rejected PCBs by the manufacturer could not be controlled.

Most artificially created scratches were intentionally made deeper and wider than those on PCBs rejected by the manufacturer, shown in Figures 8 and 9. The integrity and reliability of wire bonds made on artificially created scratches were considered a worst-case condition compared to those made on relatively shallow scratches on PCBs rejected by the manufacturer. Figures 14 and 15 show examples of scanning electron microscope (SEM) images of scratches with elemental analysis using energy dispersive spectroscopy (EDS). Figure 14 shows an example of scratches on a rejected PCB by the manufacturer during the PCB manufacturing process, and Figure 15 shows an example of scratches created intentionally for this study. The amount of gold detected on the surface of the scratched area is significantly reduced compared to that on the surface without scratches, particularly, for Figure 15. On the other hand, the amount of palladium and nickel detected on the scratched area was significantly increased since palladium and nickel were exposed to the surface. Nickel was detected significantly in some isolated areas indicated as Area 3 in Figures 14 and 15.

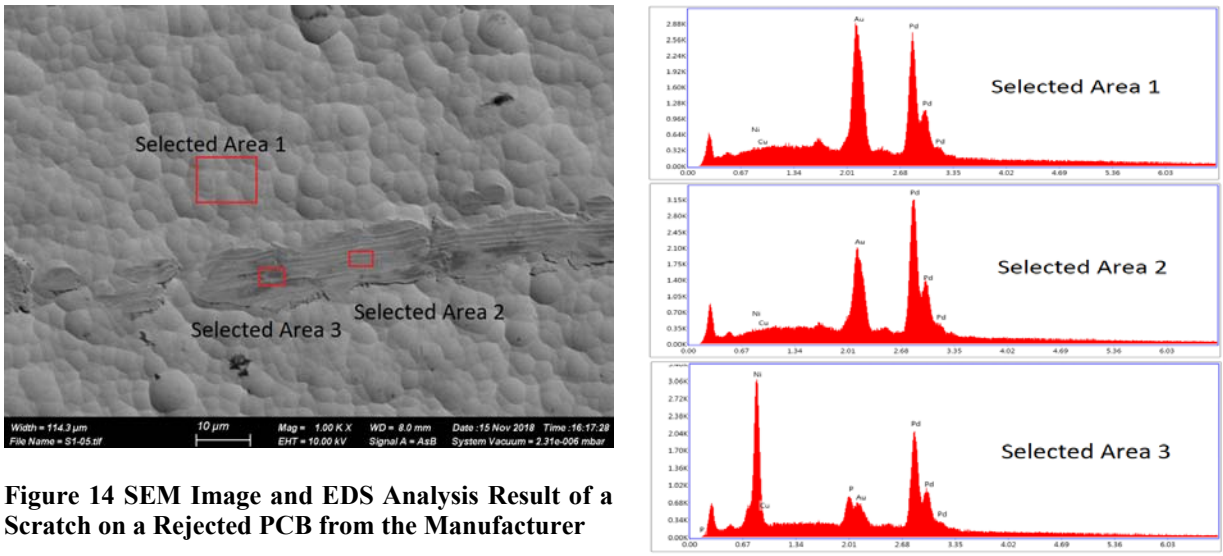
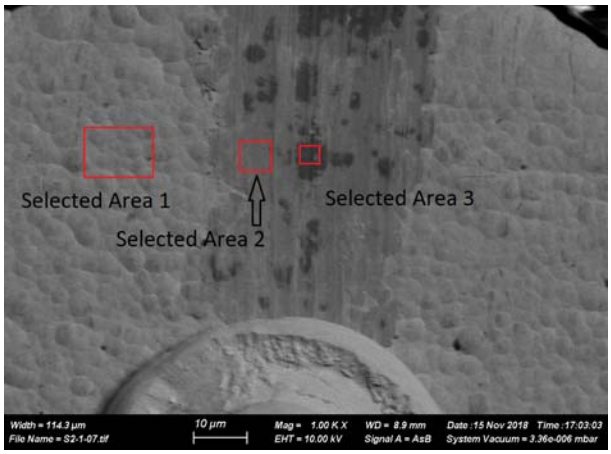


Figure 14 SEM Image and EDS Analysis Result of a Scratch on a Rejected PCB from the Manufacturer



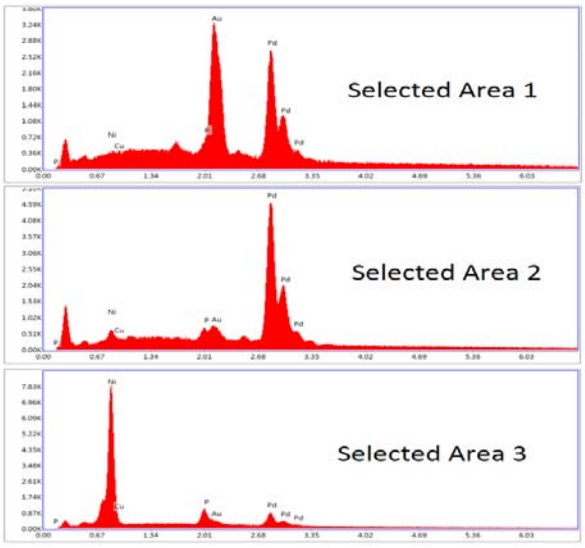


Figure 15 SEM Image and EDS Analysis Result of a Scratch Intentionally Created for This Study

There was not a way to create nodules artificially, and therefore only PCBs rejected by the manufacturer due to nodules were used. Figure 16 and Figure 17 show examples of wire bonds made on nodules and scratches, respectively. Most nodules were almost completely covered with wire bonds, so that, it was not clear if nodules were under the wire bonds.

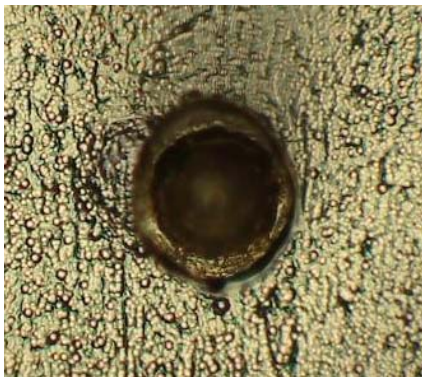


Figure 16 Wire Bond Made on Nodule

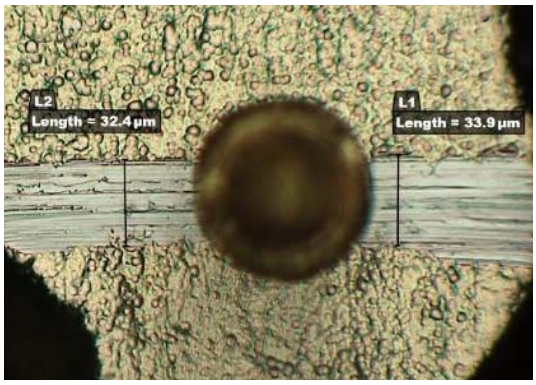


Figure 17 Wire Bond Made on Scratch

Results and Discussion of Wire Bonding Experiment

Pull test results of wire bonds made on nodules before reliability testing are shown below in Table 2. These test results are from Product I. All of the wire bonds pull tested before reliability testing showed a neck break failure mode with acceptable wire pull strength (greater than 4.0g). A neck break failure mode means that the wire bond was broken above the ball bond on the PCB bonding pad. Variation in neck break strength in Table 2 was due to the difference in wire bond length and loop height. An unacceptable failure mode would be lifted wire bonds on the PCB bonding pads instead of broken wire bonds during wire pull testing.

Table 2- Pull Test Results of Wire Bonds Made on Nodules Before Reliability Tests

PCB Product	Nodule #	Type of Nodule	Nodule Height (um)	Nodule Diameter (um)	Pull Test Failure Mode	Pull Strength (g)
Product I	N1	A	10.1	49	Neck Break	>4.0*
	N2	A	11.5	38	Neck Break	>4.0*
	N3	A	13.1	54	Neck Break	>4.0*
	N4	A	13.0	45	Neck Break	9.7
	N5	B	16.2	31	Neck Break	6.2
	N6	A	12.6	47	Neck Break	6.1

**: Pull strength was not recorded, but it was higher than the internal pull strength specification of a minimum of 4.0g.*

Table 3 shows pull test results of wire bonds made on scratches before reliability testing. Wire bonds were made on scratches on PCBs rejected by the manufacturer. Pull test results showed a neck break failure mode with acceptable pull strength.

Table 3- Pull Test Results of Wire Bonds Made on Scratches Before Reliability Tests

PCB Product	Scratch #	Scratch width (um)	Pull Test Failure Mode	Pull Strength (g)
Product I	S1	9	Neck Break	9.4
	S2	9	Neck Break	5.9
	S3	20	Neck Break	7.4

Reliability tests conducted for this study were temperature and humidity testing at 85ºC/85%RH for 300 hours, and thermal cycling test for 300 cycles in the temperature range of -40C to 85ºC. Tables 4 and 5 show the pull test results of wire bonds made on nodules after temperature and humidity testing, and thermal cycling test, respectively. Note that wire bonds made in this study were using the SSB process. Test results in this study are likely different if a standard gold bonding process or aluminum wedge bonding process had been used.

Table 4- Pull Test Results of Wire Bonds Made on Nodules after Temperature/Humidity Test

PCB Product	Nodule #	Type of Nodule	Nodule Height (um)	Nodule Diameter (um)	Pull Test Failure Mode	Pull Strength (g)
Product I	N7	A	8.3	50	Neck break	6.8
	N8	B	9.8	29x13	Neck break	6.9
	N9	A	8.7	35	Neck break	7.4
	N10	C	2.5	56x21*	Neck break	5.7
Product II	N1	A	7.8	31	Neck break	8.2
	N2	A	7.5	27	Neck break	10.6
	N3	A	8.0	28	Neck break	8.1
	N4	A	7.3	30	Neck break	8.6
	N5	A	6.5	24	Neck break	7.5
	N6	A	5.8	27	Neck break	7.1
	N7	A	6.4	29	Neck break	10.5
	N8	A	6.9	31	Neck break	6.4

**: including the size of the nick*

Table 5 - Pull Test Results of Wire Bonds Made on Nodules after Thermal Cycling Test

PCB Product	Nodule #	Type of Nodule	Nodule Height (um)	Nodule Diameter (um)	Pull Test Failure Mode	Pull Strength (g)
Product I	N11	A	7.9	44	Neck break	7.6
	N12	A	7.5	54	Stitch break	11.3
	N13	A	6.5	31	Neck break	7.5
	N14	A	4.6	35	Neck break	7.2
	N15	C	3.3	27	Neck break	8.0
Product II	N9	A	8.9	28x45	Stitch break	NA*
	N10	A	8.5	25	Neck break	NA*
	N11	A	8.7	25	Stitch break	NA*
	N12	A	7.9	32	Neck break	NA*
	N13	A	7.7	33	Neck break	NA*
	N14	A	5.6	28	Neck break	NA*

**: All the wire bonds were broken at either the neck or stitch during the removal of the frame, which is part of the product design to create a cavity in order to protect wire bonds and image sensors. Therefore, wire pull tests could not be performed. However, all the wire bonds were observed broken rather than lifted.*

Tables 6 and 7 show the pull test results of wire bonds made on scratches after reliability testing. The information about the width of the scratches are also included in the tables. The range of observed scratch widths in Tables 6 and 7 was from 17um to 33um. The widest scratch is slightly more than half of the diameter of the wire bond; however, wire pull tests after

reliability testing did not show failures. In MIL STD-883H METHOD 2010.12 [3], wire bonds made outside of the bonding pads are considered acceptable if >75% of the wire bond is within the bonding pad, which means that a maximum of 25% of the wire bond could be on a non-bondable surface. However, the area occupied by the scratch under the wire bond in this study is much more than 25%. By rough calculation, a scratch with 12.3um width would take about 25% of wire bond area of the wire bond with 63um diameter if the scratch is aligned about in the middle of the circular wire bond area. For a scratch with 33um width, the scratched area occupied under the wire bond would be about 65% of total wire bond area.

One of the reasons that wide scratches could be tolerable for the wire bonding process in this study could be that scratches did not negatively affect the surface finish wire bonding capability, as shown by the EDS results in Figures 14 and 15. Even though the gold layer was significantly damaged and removed, the pallidum layer, considered the wire bondable surface, was not completely removed. In other words, an entire scratched area may not necessarily be a non-bondable surface. This could be considered a benefit of using an ENEPIG finished surface over using an ENIG finished surface for wire bonding.

Table 6- Pull Test Results of Wire Bonds Made on Scratches After Temperature/Humidity Test

PCB Product	Scratch width (um)	Number of bonds pulled	Pull Test Failure Mode	Pull Strength (g)
Product I	19-20	1	All neck break (0 lifted bond)	Ave. 7.3 Min. 5.8 Max. 9.0 Stdev. 1.1
	20-25	4		
	25-30	5		
	30-31	2		

Table 7- Pull Test Results of Wire Bonds Made on Scratches After Thermal Cycling Test

PCB Product	Scratch width (um)	Number of bonds pulled	Pull Test Failure Mode	Pull Strength (g)
Product I	17-20	4	All neck break (0 lifted bond)	Ave. 8.0 Min. 5.7 Max. 9.4 Stdev. 1.0
	20-25	6		
	25-30	6		
	30-33	2		

Yield Analysis After Specification Update

Based on the successfully performed experiments, changes were made to the internal specification. Magnification used for inspection was reduced from 20X to 10X. Additionally, the specification was changed to allow for the presence of isolated nodules and scratches as per the criteria in the following paragraph, and Table 8.

When inspected under 10X magnification, individual nodules, such as the most commonly observed Type A and C nodules, and shallow scratches with no exposed nickel or copper in the wire bond area are considered acceptable. In some cases, process variations during PCB manufacturing, or any nodules formed from random particles that form Type B nodules may create unusual deviations resulting in exceptional nodules and scratches. In these cases, the following specification referred by Table 8 can be used.

Table 8 – Specification for Nodules and Scratches

Type of defects	Considerations	Proposed specification
Nodules	Height	Accept ≤ 15um
Scratches	Width and depth where Ni or Cu are exposed	Accept ≤ 13um width regardless of depth

Since this new specification has been applied, the yield loss at the PCB manufacturer due to nodules and scratches has shown a significant decrease over 10 months. Figure 18 shows the average yield loss due to nodules and scratches since the new specification was applied. Figure 19 shows the overview of the improvement in the average yield loss due to nodules and scratches before and after the process improvement and specification modification.

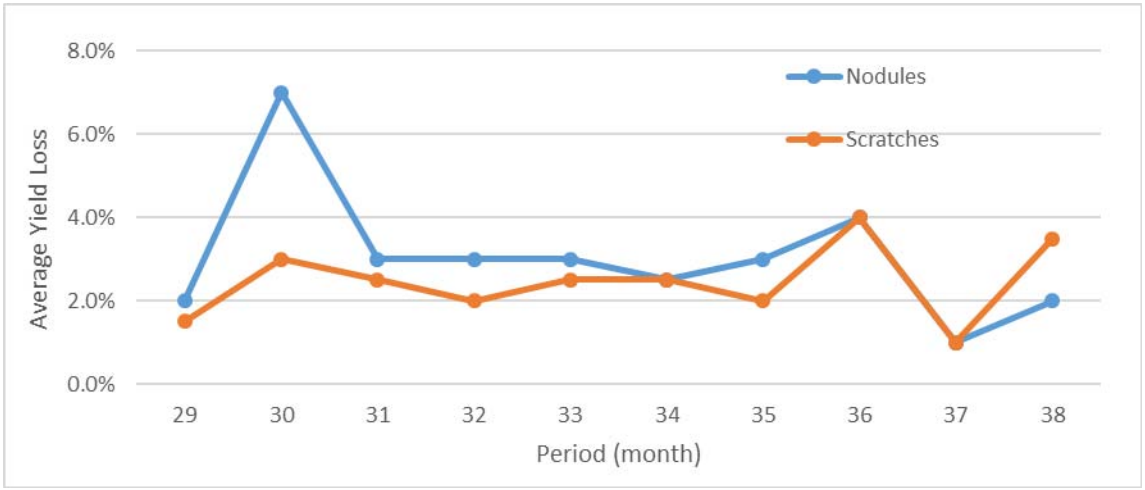


Figure 18 – Average Yield Loss with New Specification

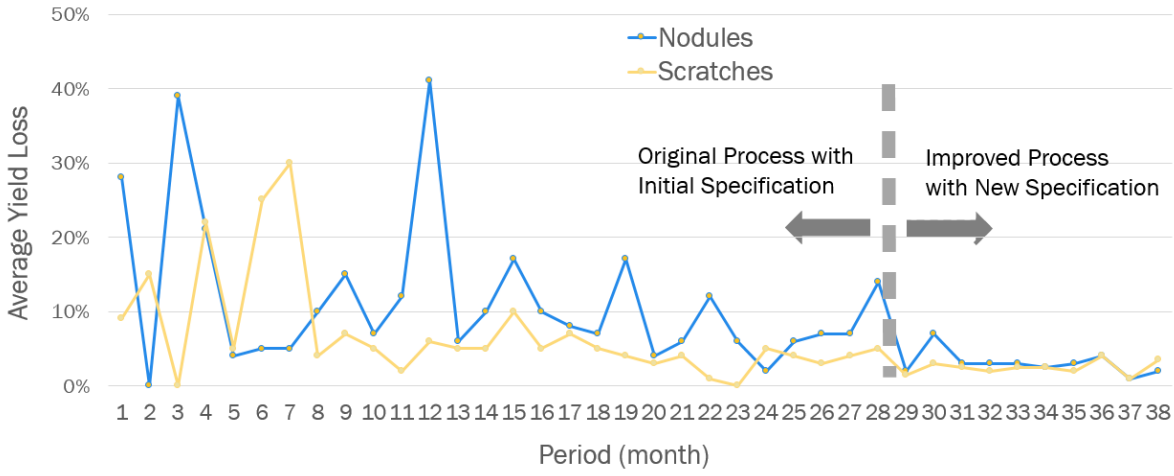


Figure 19 – Overview of Improvement in Average Yield Loss before and after Process Improvement and Specification Modification

Summary

In order to resolve significant yield loss during PCB manufacturing caused by nodules and scratches on wire bondable features, the PCB manufacturing process was improved to minimize the occurrence of nodules and scratches and wire bonds were evaluated to determine the allowable size of nodules and scratches on bonding pads for the gold wire bonding process, called SSB. Based on the wire bonding test results, the initially adopted specification, which did not allow for any nodules and scratches on any wire bondable surface, was changed to accept certain nodules and scratches, based on size and the effect on the surface finish. A summary of improvements made to the PCB manufacturing processes, the wire bonding test results on nodules and scratches using the SSB process, and the improved yield after updating the internal specification are as follows:

PCB manufacturing process

- Mechanical scrubbing after electroless copper plating for nodules was initially implemented and slightly improved yields, but later it was found that the electrolytic copper plating tank cleanliness had a more significant impact on yields.
- The cleanliness of the electrolytic copper plating tanks has been maintained through a preventative maintenance schedule to significantly reduce the occurrence of nodules.
- Foam trays with slots were implemented to transport the boards after profile routing to reduce the number of scratches.

Wire bonding on nodules and scratches

- Type A nodules were the most commonly observed nodules with a height range normally below 10um even though the height of two of them were about 13um.
- Scratches created intentionally for this study were deeper and wider (as wide as 33um) than those inflicted during PCB manufacturing. EDS analysis results showed that the gold layer was mostly removed, but the wire bondable palladium layer was only partially removed, resulting in the nickel layer only exposed sporadically.
- All the wire bonds made using the SSB process on nodules and scratches used in this study passed wire bond pull tests before and after reliability tests of temperature and humidity testing, and thermal cycling.

Yield loss due to nodules and scratches

- The internal specification was updated to address nodules and scratches on wire bond surfaces, based on the improvements made in PCB manufacturing and the results of this study. Nodules under a specific height and scratches with a certain width depending on the depth of the scratches are allowed in the new specification compared to the original specification, which had a zero tolerance for nodules and scratches.
- The average yield loss of multiple PCB products due to nodules or scratches was significantly reduced to a maximum of approximately 7% from a maximum of approximately 41%.

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References

[1] IPC-A-600, Revision J, “Acceptability of Printed Boards”, IPC, 2010.

[2] Y. K. Song, V. Bukva, “Challenges on ENEPIG Finished PCBs: Gold Ball Bonding and Pad Metal Lift”, 2016 IPC Apex Expo Technical Conference Las Vegas, NV.

[3]MIL STD-883H, METHOD 2010.12, 2010.