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ALTERNATIVE ASSEMBLY OPTIONS TO ACHIEVE COST EFFECTIVE AND RELIABLE HANDHELD PRODUCTS

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ABSTRACT

Miniaturization and the integration of a growing number of functions in portable electronic devices require a high packaging density for electronic components. One way to increase the packaging density is to reduce the size of the packages and at the same time increase the density of the I/Os. This means that the size and pitch of solder balls or pads in electronic component packages will continue to shrink.

The use of fine pitch components, equal and below 0,5mm pitch, poses a number of challenges for design, SMT assembly process and reliability.

First, a feasible assembly process must be achieved. The assembly process ranges all the way from screen-printing too in many cases underfill of CSP's and LGA's. Many factors influence the quality of the assembly process. The basic processes to control are screen-printing, pick & place, reflow soldering and underfill.

Second, the right materials (such as PCB material, PCB surface finish, solderpaste and underfill) and PCB design need to be selected to ensure a cost effective and reliable interconnect. Of coarse the mechanics of the products makes a big difference as well but it is very product dependant and many of today's products leave little room for designing the mechanics in the most reliable way due to total cost and overall looks of the product.

This paper will discuss different assembly and material alternatives to make a handheld product as producer friendly, cost effective and reliable as possible.

Key words: Miniaturization, total cost and reliability

INTRODUCTION

With the never ending drive for smaller lighter and more advanced features on handheld products the ability to handle miniaturization will be a key capability to enable these requirements.

Miniaturization can be done in many ways and this paper touch on the once that can be incorporated in a more or less standard surface mount assembly line with minimal upgrades.

The key is to ensure that several options for assembly can be achieved and this should be seen as a toolbox of technologies.

This paper will touch briefly in to several assembly options such as:

- PoP
- 0,3 and 0,4mm pitch CSP
- 0201 and 01005
- Reduced component spacing
- Interconnection methods

On the active components die stacking inside a package is one way to increase the functionality per unit area on a PCBA. However, there can be some drawbacks to creating a stacked die solution. First, this method is a customized solution. If any of the dies to be used changes, the die stack needs to be evaluated to see if changes are needed in the package. For example, a die shrink may occur which could change the whole package structure. Secondly, if one or more of the dies inside the package fail, the whole unit will have to be scraped, which would lead to increased cost; this is the well-known "compounded yield" issue. Lastly, trying to coordinate the many semiconductor suppliers to provide dies to a packaging house to do the die stacking can be a challenging task.

Package in Package (PiP) is another alternative to increase the functionality per unit area on a PCBA. PiP is similar to die stacking but instead of stacking dies, complete packages such as baseband package and memory package are stacked and then molded. This allows the memory to be fully tested before the stacking but typically gives a higher package cost than a stacked die or PoP configuration.

In the PoP process one component is placed on top of another package during a single SMT process to fully utilize the three dimensional aspect of the product. The topside of the bottom component has pads similar to the pads on the PCB for attachment of the top package. Each package is a single unit that can be fully tested as a normal

IC package is done today, so the yield would be comparable to the normal yield commonly seen today. Another advantage would be the ability to have second source options that could be fairly easily inserted into the process. The stacked package can be processed in a traditional SMT environment with a few upgrades that are readily available. Therefore, package stacking enables configurable assemblies and provides greater flexibility in the supply chain. It can be used for memory applications or processor with memory, with faster time to market and better management of package testing and compounded yield issues.

Reduced pitch is without doubt one of the bigger challenges for the active components but it is a very effective way to achieve miniaturization. Today mainstream is 0,5mm pitch but 0,4mm pitch is getting more and more popular and 0,3mm pitch is knocking on the door. Taking the step to 0,4mm from 0,5mm poses a few challenges mainly to design, screen printing and getting good quality PCB's. On 0,3mm pitch our initial studies shown that screen printing will be a big challenge and a dip fluxing process might be needed. This might sound like a big change but the process for running a inline flip chip process is more or less in place since many production lines are already using this process for PoP. The main difference would be that as of today our flip chip studies show that nitrogen will be needed to achieve high yields.

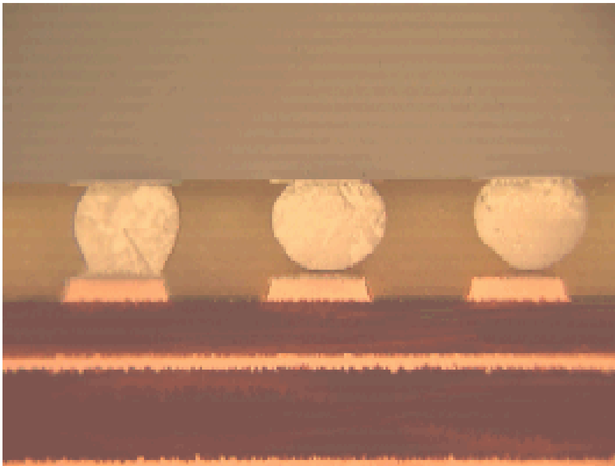


Figure 1. Reflow in air showed minimal or no collapse of the bumps.

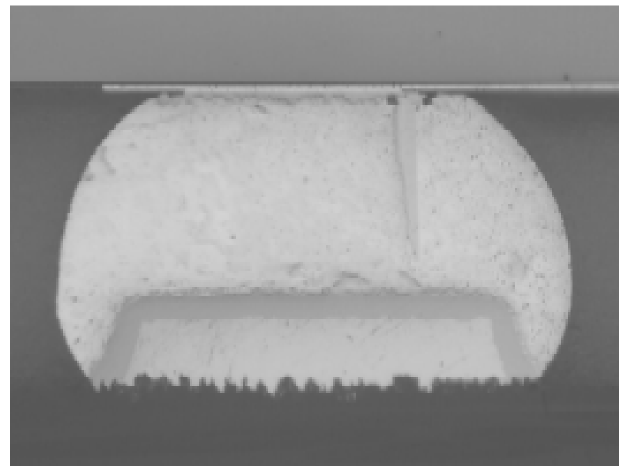


Figure 2. A good SnAgCu solder joint on ENIG that wetted fully around the pad.

With regards to passive components that are more less two ways to achieve miniaturization, smaller parts such as 0201 and 01005 and reduced spacing. Both are very much feasible but needs to be carefully considered. Considering the situation, it is not surprising that the 01005 packages are becoming increasingly interesting despite of the limited electrical values currently available, the relatively high cost and the difficulties in the production processes.

Interconnection between the main PCB and sub PCB's or FPC's is also an area where lots of space and money can be saved.

There are several methods of interconnection between two FPC's, or between a FPC and a rigid substrate such as a printed circuit board (PCB). For example, anisotropic conductive adhesives (ACA) can be used to connect FPC's to a other substrate for a variety of products such as portable music players, medical devices, and mobile phones, to replace the traditional board-to-board connectors and Zero Insertion Force (ZIF) connectors in order to decrease X, Y and Z dimensions, reduce the total cost and improve reliability.

There are basically two types of anisotropic conductive adhesives (ACA), anisotropic conductive film (ACF) and anisotropic conductive paste (ACP).

The ACF process is basically divided into two steps, pre-bonding and final bonding. In the pre-bonding process, the ACF material is transferred from a carrier tape to one of the substrates. Then the unit is transferred to the next machine (or a different station within the same machine) for alignment and the final bonding of the two units that will be attached together.

ACTIVE PARTS

This paper takes a few different test vehicles into consideration and then we have tried to map the results we are seeing on actual products.

The main board for this study was designed to be similar to a cell phone with a Package on Package structure. The panel is 186mmx108mm size (Figure 3) and each PCB in the panel is 96mmx40mm. The surface finish for this board is Organic Surface Preservative (OSP). Each of the four PCBs in the panel has different pad layouts (Figure 4) to investigate different PCB routing alternatives to achieve lower cost and/or more reliable PCB's.

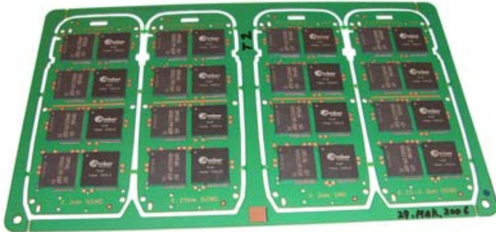


Figure 3. PCB panel, PoP.

The PCB's that are used as test vehicles has six layers using halogen-free Resin Coated Copper (RCC) in the outer layers to enable a better quality on the microvia drill. Standard FR4 is used in the inner layers. The total PCB thickness (excluding the soldermask thickness) is 1,1mm.

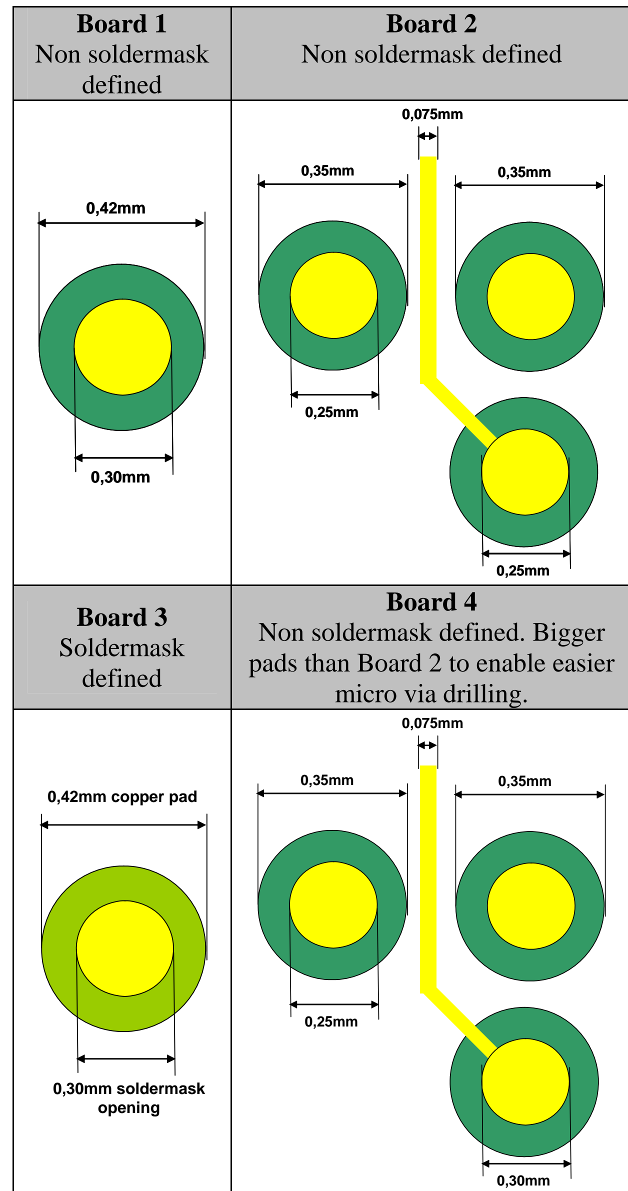


Figure 4. PCB layout.

The PoP components (Table 1) are all daisy-chained covering all balls on the top and bottom PoP.

In addition, 0201 components are placed with a spacing of 0,15mm from the PoP package and with the same distance between 0201 components.

Description	Combination A		Combination B	
	A bottom	A Top	B Bottom	B Top
Size	14x14mm	14x14mm	14x14mm	14x14mm
Pitch	0,5mm	0,65mm	0,5mm	0,65mm
Total thickness	1,4		1,5	
Number I/O	447	152	353	152
Bump size	0,3mm	0,45mm	0,3mm	0,45mm
Surface finish on component pads	Thin nickel on top and OSP bottom pad	ENIG	ENIG on top and OSP on bottom	ENIG
Bump material	SnAgCu	SnAgCu	SnAgCu	SnAgCu

Table 1. PoP Package Dimensions

Solder Paste, Flux and Underfill

A type-3 Sn95,5Ag3,9Cu0,6 solder paste was used for all our studies. The selection was made through evaluation on printability, voiding, slumping, solder balling, wetting and SIR (surface insulation resistance).

Three different no-clean tacky fluxes (A, B and C) were tested, and it has been shown that the selection of flux can have a large impact on the assembly yield. The yield difference can mainly be seen if there is a slight warpage mismatch between the top and bottom parts. As can be seen from Table 2, Flux A gave the best result.

Description	Combination A		Combination B	
	A Bottom	**A Top**	**B Bottom**	**B Top**
Flux A Solderpaste type 3	100%	100%	100%	98,86%
Flux B Solderpaste type 3	100%	100%	100%	93,75%
Flux C Solderpaste type 3	100%	100%	100%	85,42%

Table 2. Yield from the PoP Flux Screening

Reworkable, unfilled underfill materials (Table 3), with low viscosity, fast flow and fast cure, were used.

Description	Underfill A	Underfill B	Underfill C
Filler content	0	0	0
CTE	70	75	75
Tg (TMA)	65	110	10
CTE above Tg	194	165	165
Viscosity	450	250	1200
Repairable	Yes	Yes	Yes

Table 3. Underfill Material Properties

Paste Printing

The standard paste printing process was used with a 0,125mm thick laser-cut stencil. Automated solder paste inspection was done on all locations (Table 4 & Figure 5).

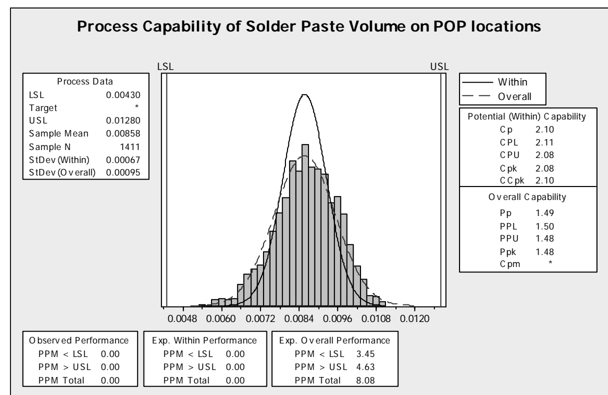


Figure 5. Solder paste Printing Cpk

Description	Mean	Standard deviation	Cp	Cpk
1 Non Soldermask defined.	590	64	1,79	1,77
2 Non Soldermask defined	595	73	1,58	1,58
3 Soldermask defined	556	68	1,70	1,51
4 Non Soldermask defined.	567	65	1,78	1,62
Overall	578	68	1,71	1,62

Table 4. Solder Paste Printing Cpk. No significant difference between the different pad layouts.

Placement and Fluxing

The bottom package, along with the other SMT components on the board, is placed first. The top part is then dipped in a 180-200um thick flux film and placed on top of the bottom package. Based on our flux screening results Flux A was used for all assemblies that were used

for mechanical and thermo mechanical reliability testing. All the assemblies were done on standard fine pitch surface mount machines equipped with a dip-fluxing unit. No assembly related defect was detected during the trials.

Reflow

A standard lead-free reflow profile was used. The reflow was done in air, with 65s above 217ºC and 245ºC peak temperature.

Figure 6. Interface between the top and bottom packages showing an intermetalic layer of 2-3um.

Figure 7. Component ball interface to the PCB pad, with an intermetalic layer of 2-3um.

Electrical Testing, X-ray and Cross-Sectioning Analyses

After reflow, all components were electrically measured for continuity and x-rayed (Figure 5) to ensure that there were no opens or solder bridges. Some opens were observed with Combination B due to a warpage mismatch between the top and bottom components. The yield can be seen in Table 2. No solder bridging was found. The smaller bottom solder joints using solder paste have more voids than the solder joints on the top solder joints using only flux. Cross-sections of the solder joints are shown in Figures 6 and 7.

Drop Test

After assembly and electrical measurement, the PCBA's were assembled into cell phone mechanics (Figure 8) and drop-tested. The drop-test was done in 3 cycles on six sides giving in total 18 drops from 1,5m. 48 parts were tested for each combination (Table 5). All the failures occurred at component locations under the battery. Four different failure modes were observed in the failure analysis (Figures 9-14).

1. PCB cracking in the RCC dielectric layer with the non-soldermask defined pads.
2. Cracks in the intermetalic layer between the solder bump and the PCB copper pad on the soldermask defined pads.
3. Cracks in the intermetallic layer between the solder bump and the component copper pad.
4. Cracks at the IMC–nickel layer interface at the topside of the bottom component pad, between the top and bottom components. This failure mode was only found on the Combination B with the ENIG component pad surface finish.

Figure 8. Basic structure of the cell phone used for the drop-testing.

Description	Combination A		Combination B	
	A Bottom	A Top	B Bottom	B Top
No underfill Layout 1 NSMD	4/48	No failure	3/48	4/48
Underfill A Layout 1 NSMD	No failure	No failure	No failure	No failure
Underfill B Layout 1 NSMD	No failure	No failure	No failure	No failure
No underfill Layout 3 SMD	5/48	No failure	1/48	2/48
Underfill B Layout 3 SMD	No failure	No failure	No failure	No failure
Underfill B Layout 3 SMD	No failure	No failure	No failure	No failure

Table 5. Drop-test results, PoP.

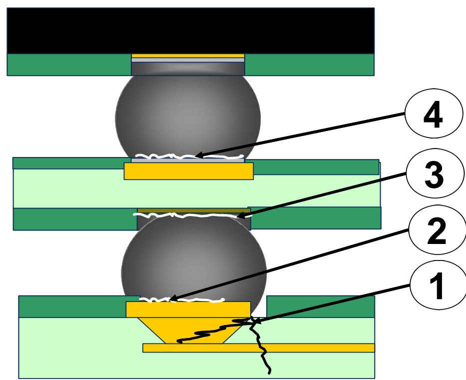


Figure 9. The four different failure modes seen on the PoP components.

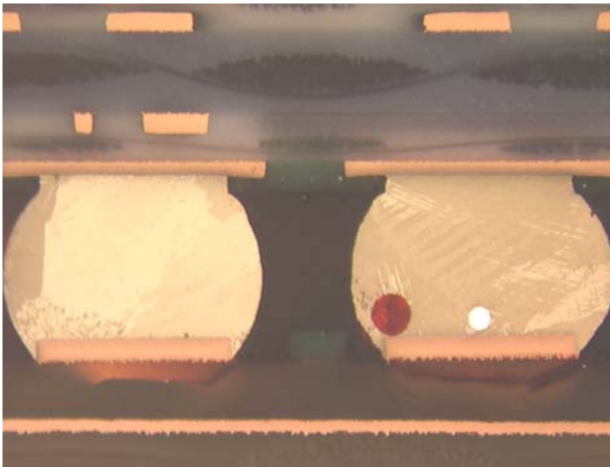


Figure 10. Failure mode 1: PCB cracks in the RCC dielectric layer with the non-soldermask defined pads.

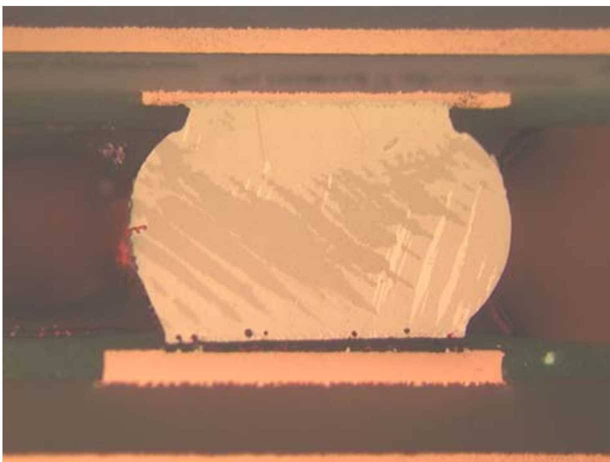


Figure 11. Failure mode 2: Cracks in the intermetalic layer between the solder bump and PCB copper pad on the soldermask defined pads.

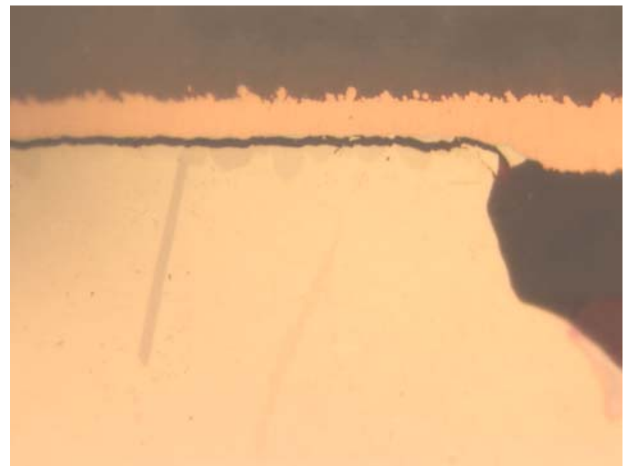


Figure 12. Failure mode 3: Cracks in the intermetallic layer on the bottom component pad on package.

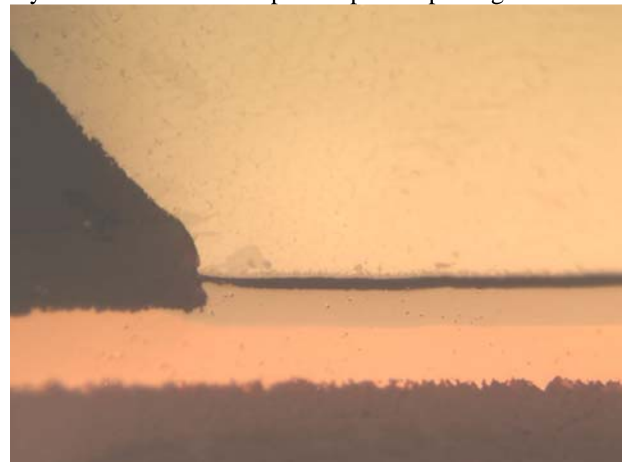


Figure 13. Failure mode 4: Cracks at the IMC–nickel layer interface of the topside of the bottom component pad on combination B. This failure only occurs with Combination B.

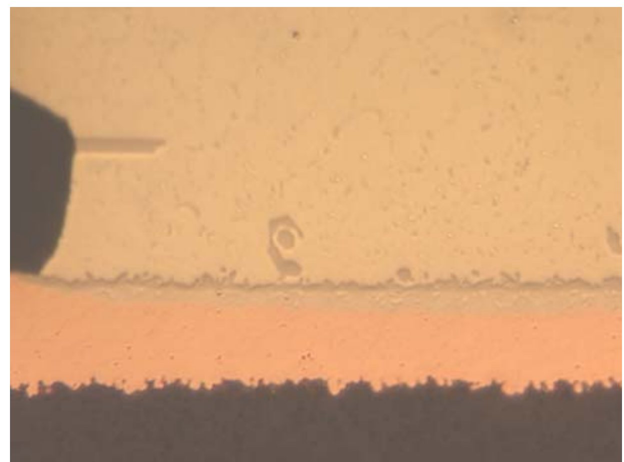


Figure 14. Failure mode 4 was not observed with the thin nickel finish in Combination A.

The results from the drop test of PoP is very similar to what we see in product level testing with PoP and also other type of CSP's such as 0,4mm pitch CSP's.

The smaller the pad the bigger the risk is for PCB cracks during mechanical stress.

The poor adhesion between copper and PCB material also create an extra challenge during rework and the risk of getting so called pad lifts leading to a scrapped PCBA is high.

Due to the above a soldermask defined pad might be a better solution on fine pitch CSP parts. Our data so far shows more or less the same reliability data for a non soldermask defined pad and a soldermask defined pad but rework is easier with the soldermask defined pad.

An other advantage of using a soldermask defined pad on a 0,4mm pitch CSP is that the microvia drilling will be much easer and that the soldermask sliver between two pads will be approximately 0,15mm instead 0,05mm reducing the risk of solder bridging.

The main risk with the soldermask defined pad is controlling the soldermask thickness on top of the pad.

Thermal Cycling

After assembly and electrical measurement a number of them went through thermal cycling -40-85°C for 800 1h cycles, results can be seen below in table 6.

Description	Combination A		Combination B	
	A Bottom	A Top	B Bottom	B Top
No underfill	No failure	No failure	No failure	No failure
Underfill A	No failure	No failure	2/8	8/8
Underfill B	No failure	No failure	No failure	4/8
Underfill C	No failure	4/8	6/8	7/8

Table 6. Thermal cycling results after 800 cycles, PoP.

Figure 15. Thermal cycling cracks on top part combination B with underfill C.

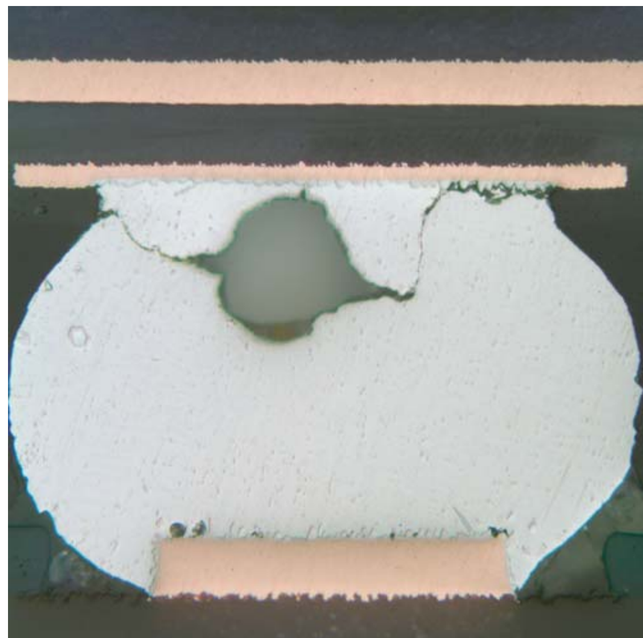


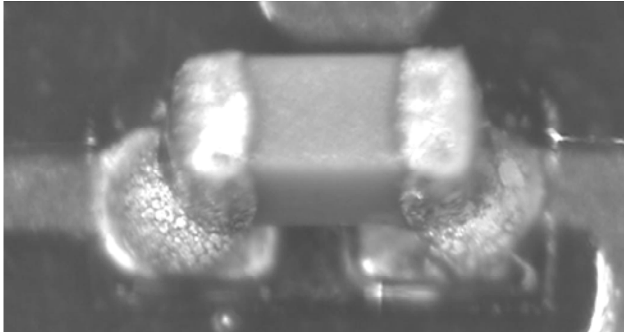
Figure 16. Thermal cycling cracks on bottom part combination B with underfill C.

PASSIVE COMPONENTS

This paper takes a few different test vehicles into consideration and then we have tried to map the results we are seeing on actual products.

Our data clearly show that reduced spacing and 01005 are feasible if the right preparation work is done. Reduced spacing is more of a “plug inn” solution compared to 01005. Our data show that a 3mil thick stencil and a type 5 solderpaste is needed for 01005 and this will have an impact of the rest of the surface mount process. The main challenges with 01005 is printing and reflow and once the

optimum pad layout is achieved for screen printing the reflow profile need to be optimized to eliminate so called dry solder that is a direct effect of excessive preheating/soak. Our studies shown that with the right solder paste selection and reflow profile nitrogen is not needed to achieve high yields.



Picture 17. Result of excessive preheating

From a spacing point of view it is important to base this on data and based on our data we see a clear breakpoint and 0,15mm spacing. In the figure below we have combined a number of different combinations but the trend is clear that 0,15mm is a breakpoint for achieving high yields. Some part might be placed tighter but this needs to be done on a case by case basis.

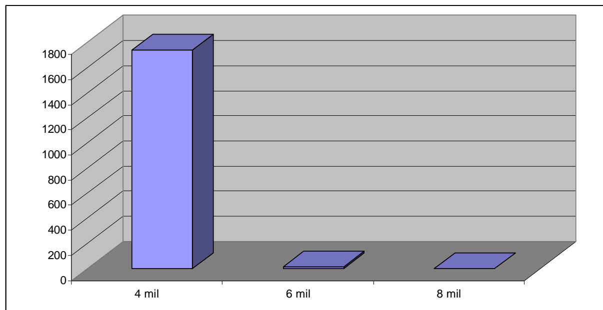


Figure 18. DPMO at different component spacing.

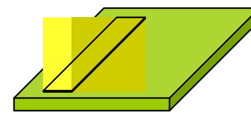
INTERCONNECTION METHODS

Three different test boards, all with a size of 22,1x12mm where created to be able to study FPC/FPC ACF bonding and FPC/PCB ACF bonding , the pitch is 0,2mm with 88 connections. The copper trace width and trace spacing is 0,1mm. Compared to using connectors this is a very tight pitch and can potential eliminate one layer in the on the FPC giving an overall lower cost.

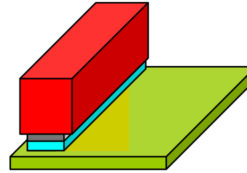
Process Flow

The ACF process can basically be separated in to two different steps, pre-bonding and final bonding (Figure 19a and 19b).

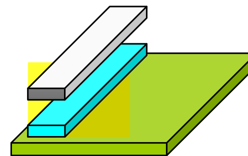
No cleaning was done on the ACF bonding pads before bonding.



Put the FPC or PCB into a fixture. The sustrate is secured with vacuum.

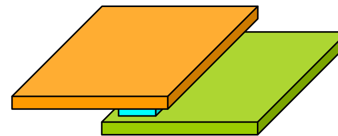


Apply the ACF film and pre-bond it to the substrate. Typical bondline temperature is 90ºC for 1s with a 1Mpa pressure.

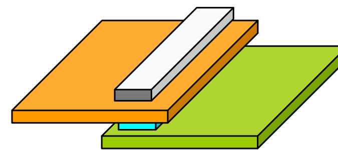


Remove the protective ACF film and inspect.
The protective film is removed automaticly by the machine.
Once inspection is done transfer to the final bonding step

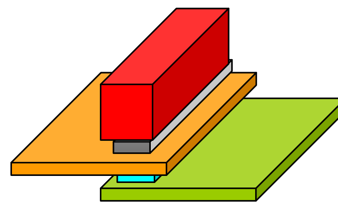
Figure 19a. ACF pre-bonding process flow.



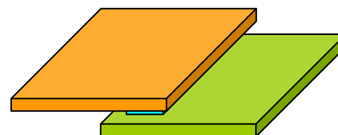
Put both substrates into the fixure and align them. Both sustrates is secured with vacuum.



Rotate the fixture into bonding position.
The compliant rubber and bond heat will be aligned to the bonding loction.



Perform final bonding.
The typical bond line temperature is 140-210ºC for 10s with a pressure of 2-4Mpa



Bonding finished.
Remove from fixture and inspect under a microscope.

Figure 19b. ACF final bonding process flow.

The actual bonding area is 22,1x6mm but in this study we used a bonding area of 22,1x2mm.

The surface finish for all boards is electroless nickel with immersion gold and further studies will be done with OSP

as surface finish to be able to reduce the FPC and PCB cost.

The FPC and PCB have one copper layer. The total FPC thickness is 0,1mm and the rigid PCB is 0,6mm thick.
The FPC is made of polyimide with a polyimide coverlay and the PCB is made of FR4 a standard soldermask.

ACF material selection
Four different repairable ACF materials (A, B, C and D, Table 7) were tested, and it has been shown that the selection of ACF will have a big impact on yields and reliability.

The selection of materials was made through a detailed study and evaluation looking at process performance, cost and thermal & mechanical reliability testing.

The ACF application was presented to a number of different material suppliers and the suppliers made their recommendations based on our application requirements. Once the material recommendation was given from the suppliers we picked four materials for our testing.

	ACF materials			
Description	**A**	**B**	**C**	**D**
ACF width	1,5mm	1,5mm	1,5mm	1,5mm
Particle type	Ni core plated with gold	Ni core plated with gold	Ni plated with gold on polymer core	Ni core plated with gold
Particle size	8um	10um	10um	2um
Adhesive thickness	40um	35um	35um	35um
Reworkable	Yes	Yes	Yes	Yes

Table 7. ACF Material Properties

All ACF material performed well from a themal cycling point of view and material C was chosen as a production material based on it superior peel test performace.

	ACF materials			
	A	**B**	**C**	**D**
Thermal cycling -40-85°C 800 cycles	No failure	No failure	No failure	No failure

Table 8. Thermal cycling results after 800 cycles, ACF.

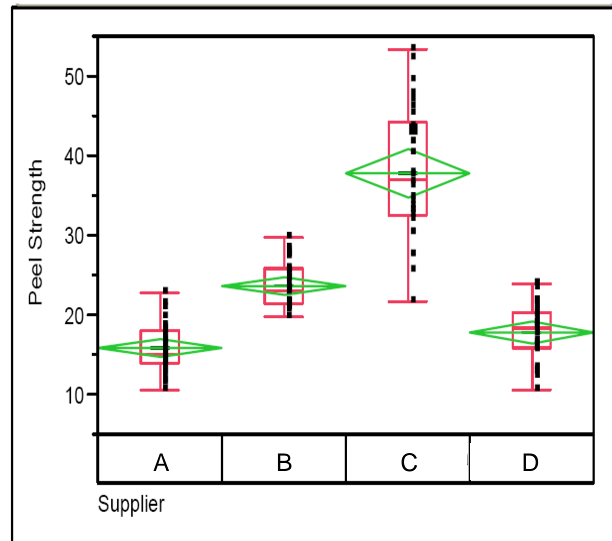


Figure 20. Peel test results.

CONCLUSIONS
There are many ways to achieve miniaturization and the key is to have a "tool box of technologies" to be able to fulfill the needs. Depending on the product several options can be considered and the selection should be based on data on assumptions.
In addision to the technologies mentioned in this paper there are other technologies such as hotbar soldering, integrated active and passive parts and COB with wire bonding that could be interesting for a miniaturization and cost point of view.

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