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Achieving Solder Reliability for LGA Ceramic Image Sensors Through Refinement of SMT Soldering Processes

Lynda Pelley, Teledyne DALSA Inc., Waterloo, ON, Canada
Hugo Gallegos, SMTC Inc., Chihuahua, Mexico

Abstract
New product introduction at an Original Equipment Manufacturer (OEM) typically includes reliability testing in the form of thermal cycling. Samplings from the engineering models of a new product line were consistently failing the optical testing following the reliability testing. Cross sectioning revealed stress fractures in the solder joints of the LGA ceramic image sensor component. As the image sensor dominates one side of the PCA, the root cause appeared to be Coefficient of Thermal Expansion (CTE) mismatch between the FR4 material of the PCA and the ceramic body of the image sensor. As this new product line was to be high volume, the goal was to avoid introducing an additional component under fill process step and resolve reliability issues through basic SMT assembly processes at the Contract Manufacturer (CM).

A joint OEM-CM Tiger Team explored the contributions of both the solder paste volume and the reflow temperature profile to the robustness of the LGA solder joints. The stencil design aspect included the shape of the aperture and the resulting volume of solder paste deposited. The solder paste volume affects the standoff of the component from the PCA. The sensor manufacturer datasheet for the oven reflow profile allowed a range of temperature values, the most significant being the temperature cool down slope. The cool down slope affects the granularity of the solder joint. The CM's team performed a DOE maximizing and minimizing both the solder paste volume and the temperature profile cool down slope combinations.

The DOE results trended towards higher paste volume and steeper temperature cool down slope. The risk of solder bridging using the higher paste volume was minimal, but the steeper temperature cool down slope produced unacceptable process voids. Therefore, the choice for optimal SMT process condition was a combination of high solder volume and lower temperature cool down slope. Passing results for optical testing post reliability testing, followed by cross section, validated this optimization.

Introduction
Reliability testing performed as part of new product introduction included thermal cycling to simulate long-term reliability of the soldering. For this product, the temperature range was -40°C to 85°C, with a cycle consisting of 15 minutes at low temperature, 5°C/minute rise for 25 minutes, 15 minutes at high temperature, 5°C/minute fall for 25 minutes, and repeated for 300 cycles. This testing simulates reliability for 8.6 years based on IPC-SM-785 and IEC 60068-2-14. The product was not powered during the thermal cycling. Following the reliability test, the product's image sensor underwent optical testing. A significant number of the test samples failed.

Investigation
Based on the failure mode during the optical testing, the issue appeared to be open or intermittent solder joints on the LGA sensor. The initial investigation step was to perform a dye and pry on one of the failed samples to determine the optimal locations for cross section. Based on the dye and pry, the weakest solder joints were as indicated in Figure 1 and Figure 2.

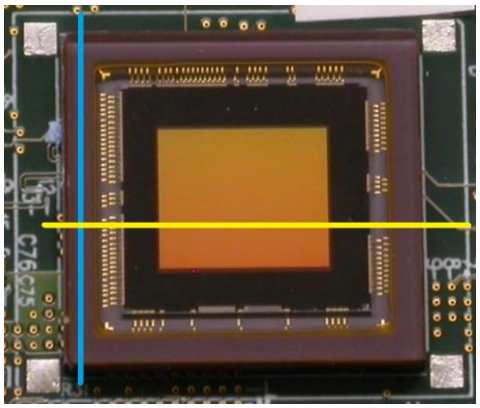

Figure 1 – Cross Section Locations Component

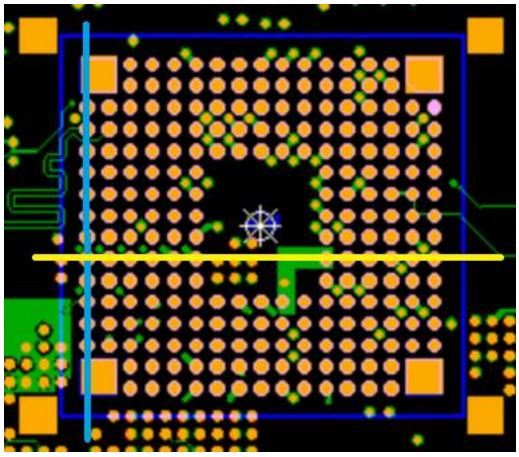

Figure 2 – Cross Section Locations Layout

The trend for cross section results was complete cracks in the solder joints nearest to the outer corners (Figure 3) and some partial cracking on the solder joints further in from the edges and corners (Figure 4). The sharp structure within the cracks indicates grain coarsening in the solder joints.

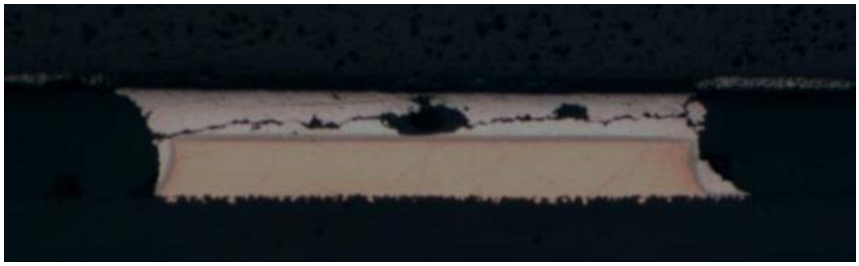

Figure 3 – Complete Crack Example, Outer Corner Locations

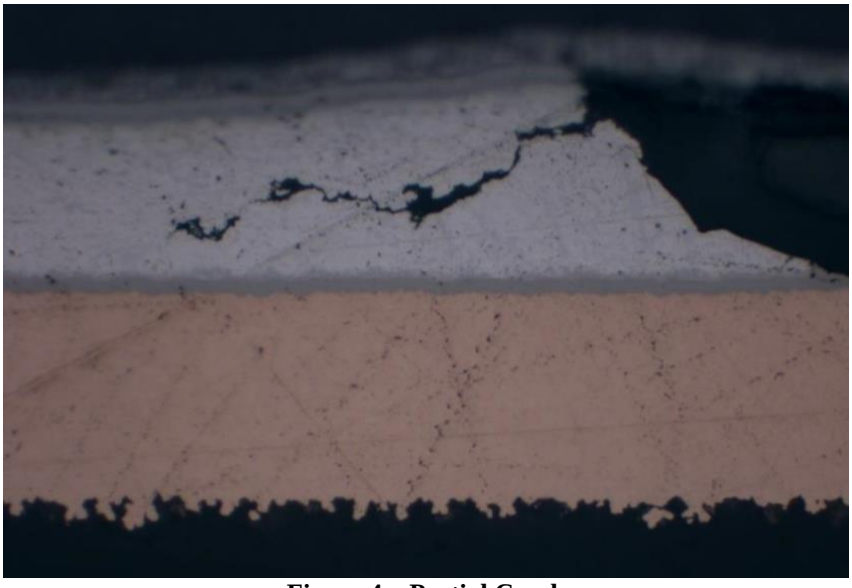

Figure 4 – Partial Crack

Other than the cracking, the cross sections confirmed that the wetting of solder to PCB was excellent and the Inter-Metallic Compound (IMC) was contiguous and normal, with no nickel dissolution.

The production parameters associated with these results:
PCB finish: Electroless Nickel Immersion Gold (ENIG)
Solder type: SAC 305, M17, Mesh size 4
Stencil thickness: 4.5 mils

Stencil aperture: Round aperture split by half, no diameter reduction
Volume of paste deposit: 1550 mil^3
Thermal profile: Ramp-Soak-Spike, pre-heat slope +1.7°C/second, Time-Above-Liquidus (TAL) from 217°C 56.3 seconds, Peak temperature 240.68°C, Cool down slope -1.43°C/second.

Design of Experiments (DOE)
The goal of the DOE was to explore the contributions of the solder joint volume and the reflow oven temperature profile cool down slope to the robustness of the solder joint to withstand reliability testing. All other soldering variables would remain the same.

For the solder joint volume, two stencil apertures were chosen to represent a low and high parameter. The low volume aperture would be the baseline used previously and the high volume aperture would test for possible increased mechanical strength and higher standoff to withstand CTE mismatch and possible materials warping. The risk associated with increasing the paste volume is solder bridging between LGA pads under the component.

Low parameter: Round aperture split in two halves, no diameter reduction, volume 1550 mil^3
High parameter: Square aperture split in two halves, overprint corners on solder mask, volume 2246 mil^3

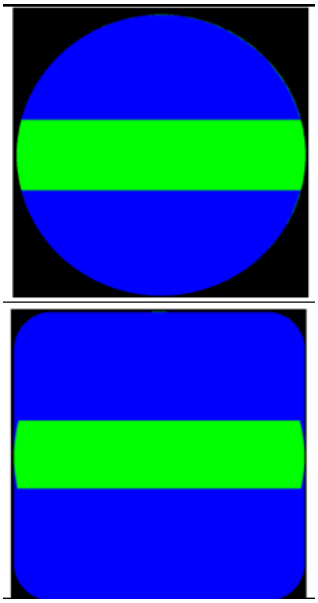

Figure 5 – Stencil Aperture Shapes; Blue is Aperture and Green is Pad

The PCB panel layout is 8-up, 2x4, as per Figure 6. The stencil design included both apertures, such that one 2x2 section used the low volume aperture and the other 2x2 section used the high volume aperture, as per Figure 7.

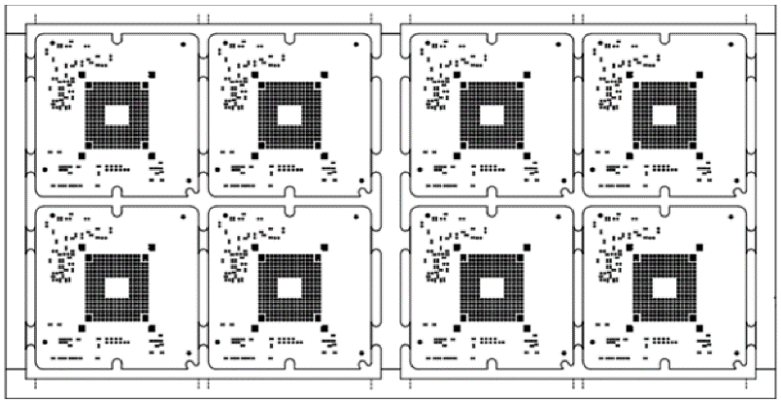

Figure 6 – PCB Panel Layout

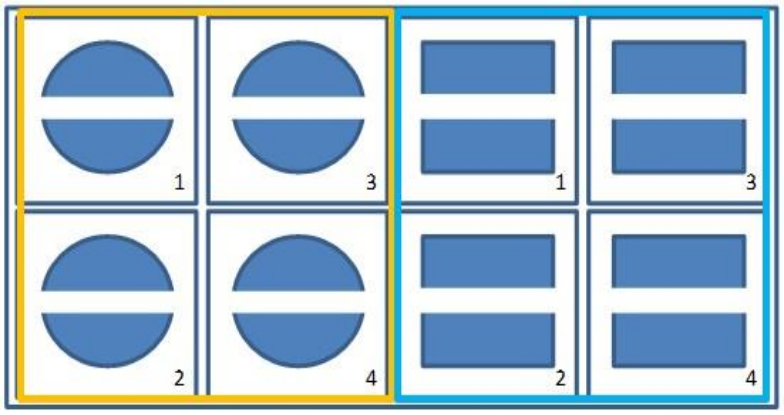

Figure 7 – Stencil Apertures for LGA Sensor Applied to PCB Layout

For the reflow oven temperature profile, the thermomechanical response of the Sn content of the SAC305 alloy was considered. As Sn is anisotropic, the size and orientation of the grain structure contributes to CTE mismatch fractures along the larger axis of a solder joint, laterally rather than vertically. The grain of the Sn present in the solder joint grows during the reflow and continues to grow during the cooling. The cool down slope is an important parameter to control grain size such that it will not provide a media for crack propagation nor be the cause of a crack starting.

Two cool down slopes were chosen to represent a low and high parameter, Figure 8. To reduce the grain coarsening of the Sn, the cool down must be accelerated, at least during the first cooling zone, to reach approximately 170°C. The process window in this zone goes from -1°C/second through to -4°C/second for cooling. The risk associated with increasing the cool down slope is voids in the solder joints.

Low cool down slope parameter: -1.8°C/second
High cool down slope parameter: -3.4°C/second

Figure 8 – Oven Cool Down Zones, Left -1.8°C/second, Right -3.4°C/second

The DOE was performed combining the two variables, A-Stencil Aperture and B-Profile Cooling Rate, as per Table 1. This provided a sample size of 4 boards soldered with each combination.

Table 1 – DOE $2^K=2^2$, Two Variables, Two Levels

Panel #	Stencil Aperture	Stencil Aperture	Profile (Cooling Rate)
1	A Low	A Low	B Low (1.8 °C/sec)
1	A Low	A Low	B Low (1.8 °C/sec)
1	A High	A High	B Low (1.8 °C/sec)
1	A High	A High	B Low (1.8 °C/sec)
2	A Low	A Low	B High (3.4 °C/sec)
2	A Low	A Low	B High (3.4 °C/sec)
2	A High	A High	B High (3.4 °C/sec)
2	A High	A High	B High (3.4 °C/sec)

DOE Results

Solder shorts, identified by x-ray inspection, were considered as a risk for the overprinted square stencil aperture (A1-A4 High). A solder short appeared on only one of the samples, and it was with the round stencil aperture, not considered to be a risk for shorts. This was likely a random anomaly, not related to the DOE test conditions. Since none of the samples with the high volume solder condition had solder shorts, the risk of using the overprinted square stencil aperture was considered acceptable.

Voids, identified by x-ray inspection, were considered as a risk for the higher cooling rate of the solder reflow temperature profile. This risk was justified, as all of the High Cooling Rate samples failed x-ray inspection for having voids in the solder joints greater than 30%.

The optical testing was performed at every interval of 100 thermal cycles. Since all DOE combinations passed the optical testing after 300 thermal cycles, the trial was extended to 400 thermal cycles to observe if a failure pattern would emerge. Based on the optical testing, there was no failure pattern. Each of the combination sets had one board of the four fail.

Table 2 – Summary of DOE Results

Card	Panel #	Serial Number SCU0219	Stencil Aperture	Cooling Rate	Solder Shorts	Voids (<30%)	100 Thermal Cycles	200 Thermal Cycles	300 Thermal Cycles	400 Thermal Cycles	Solder Quality
1	1	Scrap	A1 Low	B Low 1.8°C/s	Fail	Pass	N/A	N/A	N/A	N/A	N/A
2	1	02187	A2 Low	B Low 1.8°C/s	Pass	Pass	Pass	Pass	Pass	Pass	Fail
3	1	02185	A3 Low	B Low 1.8°C/s	Pass	Pass	Pass	Pass	Pass	Pass	Fail
4	1	02197	A4 Low	B Low 1.8°C/s	Pass	Pass	Pass	Pass	Pass	Fail	Fail
5	1	02196	A1 High	B Low 1.8°C/s	Pass	Pass	Pass	Pass	Pass	Pass	Pass
6	1	02198	A2 High	B Low 1.8°C/s	Pass	Pass	Pass	Pass	Pass	Fail	Pass
7	1	02192	A3 High	B Low 1.8°C/s	Pass	Pass	Pass	Pass	Pass	Pass	Pass
8	1	02184	A4 High	B Low 1.8°C/s	Pass	Pass	Pass	Pass	Pass	Pass	Pass
9	2	02186	A1 Low	B High 3.4°C/s	Pass	Fail	Pass	Pass	Pass	Fail	Fail
10	2	02188	A2 Low	B High 3.4°C/s	Pass	Fail	Pass	Pass	Pass	Pass	Fail
11	2	02195	A3 Low	B High 3.4°C/s	Pass	Fail	Pass	Pass	Pass	Pass	Fail
12	2	02190	A4 Low	B High 3.4°C/s	Pass	Fail	Pass	Pass	Pass	Pass	Fail
13	2	02194	A1 High	B High 3.4°C/s	Pass	Fail	Pass	Pass	Pass	Fail	Pass
14	2	02189	A2 High	B High 3.4°C/s	Pass	Fail	Pass	Pass	Pass	Pass	Pass
15	2	02193	A3 High	B High 3.4°C/s	Pass	Fail	Pass	Pass	Pass	Pass	Pass
16	2	02182	A4 High	B High 3.4°C/s	Pass	Fail	Pass	Pass	Pass	Pass	Pass

The Solder Quality column in Table 2 summarizes the results of the cross sections. The cross sections were performed after 400 thermal cycles were completed, and revealed trends that the optical testing could not. The optical testing would pass if the solder joints were only partially cracked and remained electrically connected. The majority of the solder joints that fractured were located along the exterior row, compared to the middle row sectioned. For example, 46 solder joints from the outer rows exhibited either partial or complete cracks compared to 12 solder joints with partial or complete cracks from the middle rows.

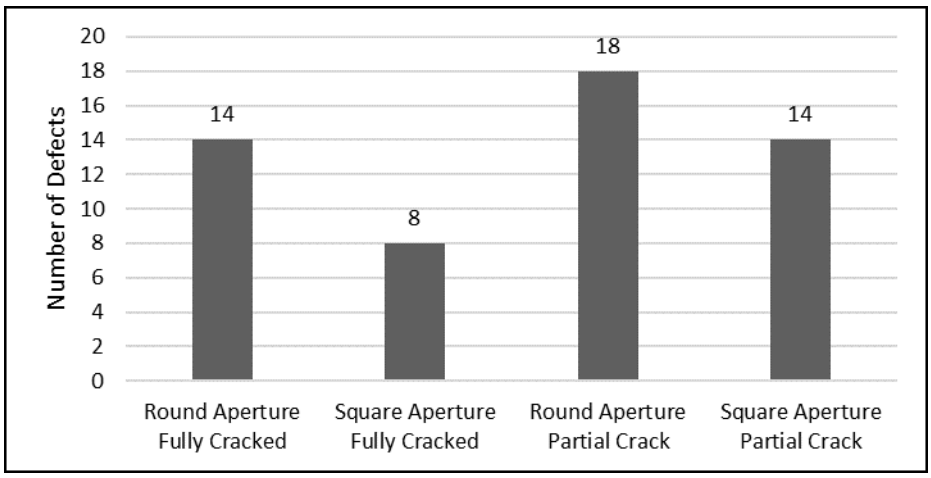

Figure 9 – Solder Joint Cracking per Stencil Aperture Type

Figure 9 identifies the trend of fewer solder joint cracking defects with the higher solder volume square stencil aperture. Based on the cross section results and the lack of solder shorts, the overprinted square aperture is the preferred stencil design.

The cross section results also identified the impact of the oven reflow temperature cool down slope. The low cool down slope had thicker IMC compound and therefore increased risk of grain coarsening, but was still acceptable with excellent wetting. Table 3 provides a comparison of the IMC thickness for both the LGA and a BGA component for 2 opposite DOE conditions.

Table 3 – IMC Thickness Comparison

Serial Number	IMC to PCB	IMC to LGA	IMC to PCB	IMC to BGA	Stencil	Cooling Slope
SCU021902186	40-140 µin	30-100 µin	20-100 µin	30-40 µin	Low	High
SCU021902192	40-120 µin	70-100 µin	60-100 µin	40-90 µin	High	Low

Although the higher cool down slope is preferred to minimize grain coursing based on average IMC thickness, the lower cool down slope provides acceptable results. In addition, the solder joints with the higher cool down slope had unacceptably large voids that increase the risk of cracking. Therefore overall, the lower cool down slope was preferred for the oven reflow temperature profile.

Conclusion

Based on the DOE, the stencil aperture design has more influence on overcoming CTE mismatch between the ceramic LGA and the FR4 PCB than the reflow oven temperature profile cool down slope. Considering the results of the DOE and the identified risks with each approach, the overprinted square stencil aperture and the lower temperature cool down slope 1.8°C/second was chosen for the process design. The NPI was successful. Post DOE and engineering trials, there have not been any further CTE mismatch issues with the regular production of this product.

References

IPC-SM-785: Guidelines for Accelerated Reliability Testing of Surface Mount Attachments
IEC 60068-2-14: Environmental Testing of Electronic Equipment; Tests – Test N: Change of Temperature

Acknowledgements

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