STENCIL PRINTING TECHNIQUES FOR CHALLENGING HETEROGENEOUS ASSEMBLY APPLICATIONS

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ABSTRACT
The challenges associated with stencil printing of miniaturized components in heterogeneous assembly are well documented with proven printing solutions [1]. Now with the reality that the ultra-small Metric 0201 passive component is being introduced to market, printing capability is once again not assured. A series of focused Metric 0201 experiments investigating printing process sensitivity to circuit board properties, including pad dimensional accuracy and landscape topography, identified stencil gasket as significantly important on achieving print process control. The effects of pad size influencing print quality were found to be less using a nano-coated stencil. The print quality produced on undersized Cu pads was significantly degraded with an un-coated stencil, whereas full Cu pads printed better. The stencil with an applied nano-coating improved print volume uniformity on all Cu pad sizes more significantly than improving overall paste transfer efficiency. Based on this test, the recommended print process used an 80µm thick nano-coated foil, which outperformed a 50µm thick stepped stencil of equivalent aperture size.

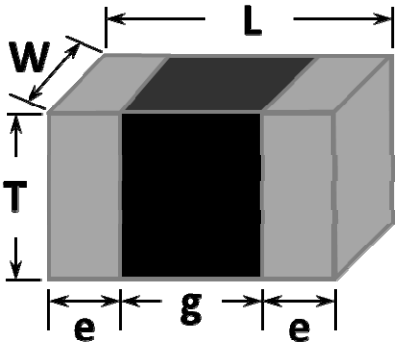
Key words: 0201, 008004, passive, fine pitch, stencil printing, nano-coating, miniaturization

INTRODUCTION

A new generation of near microscopic size SMT chip capacitors has appeared in the market, known as either 0201 (Metric dimension label) or 008004 (Imperial dimension label). Assembly results using these components is so far largely obscured from publication and highly proprietary. All aspects of the assembly process are expected to be challenged to accommodate the extreme level of miniaturization embodied in this device. The objective of this research is to investigate and characterize the stencil printing process for compatibility with M0201 (Metric 0201) capacitor assembly. Effects of circuit board quality, stencil thickness, and stencil nano-coating are the primary experiment variables reported against solder paste volume transfer efficiency and raw volume print distribution.

M0201

The designation "M0201" implies a case size length of 0.2mm and width of 0.1mm, when in fact these are actually produced at nominal dimensions of 0.25mm x 0.125mm (Figure 1).



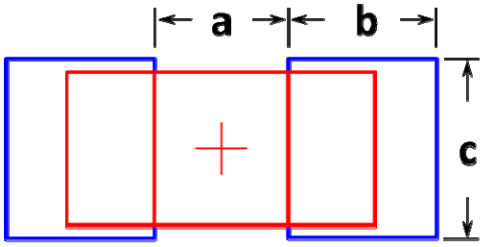
Murata GRM Series (all dimensions in microns)

L	W	T	e	g
250	125	125	50 - 100	50
@ ± 13	@ ± 13	@ ± 13		@ min.

Figure 1. M0201 Capacitor Dimensions & Tolerances [2]

In a footprint area comparison, the M0201 covers only 39% of a M0402 (Imperial 01005) chip component. M0201 capacitors were first commercially available for volume prototype assembly testing in 2014[3]. Resistor M0201 passives are not yet known to be offered.

PCB land design options for M0201 are shown in Figure 2 as prescribed by the component manufacturer. The smallest pad size is 125µm x 70µm, which approximately matches the metal end terminal footprint. The largest pad size nearly doubles the smallest pad size area at 145µm x 120µm.



Pad Outline = Blue
Component Outline = Red

Murata GRM Series (all dimensions in microns)

L/W Code	Chip L x W	a	b	c
01	250 x 125	100 - 110	70 - 120	125 - 145

Figure 2. M0201 Vendor Pad Size Recommendations [4]

The pad design of our preference is shown in Figure 3, which is at the top limit of the suggested pad size range. The motivation for using such sizeable pad dimensions include:

- Over etched Cu is expected to be problematic at this dimensional scale. Using the largest Cu pad design should at least help to improve PCB manufacturability.
- Typically the stencil aperture size mimics pad the dimensions. The largest pad area offers to ease aperture area ratios and permits potentially improved print volume control.

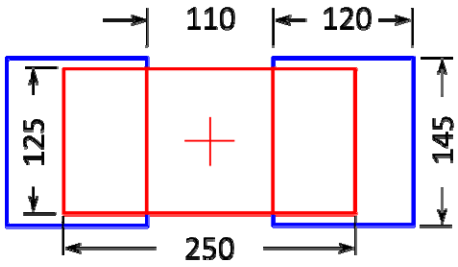


Figure 3. Selected M0201 Pad Design for Print Study

PREREQUISITE SOLDER VOLUME

The determination of a suitable stencil aperture capacity requires prerequisite knowledge of the appropriate reflowed solder joint form. The IPC-A-601E standard was consulted as an appropriate reference to determine this [5]. Figure 4 illustrates the model used to establish the structure of an acceptable M0201 solder joint of minimum volume. See associated Table 1 for legend. Author judgment prevailed for dimensions not explicitly provided in the 601E standard. The determination of this smallest solder volume is helpful in establishing a stencil design and for evaluating print performance against solder paste inspection (SPI) data.

Table 1. Label Definitions for Figure 4

D = Side Joint Length = 70µm
H = Termination Height = 125µm
F♣ = Min. Fillet Height = G + (25% H) = 46µm
G♦ = Solder Thickness = 15µm
L = Pad Length = 120µm
P = Pad Width = 145µm
U = Side Joint Width = 10µm
V = Solder Joint Volume
W = Termination Width = 125µm
Y♠ = End Joint Width = 26.7µm

♣ IPC-A-601E, 8.3.2
♦ Based on cross sectioned examples
♠ Author specified

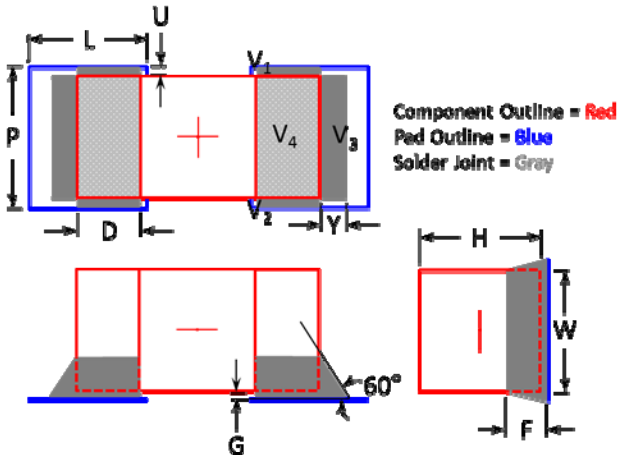


Figure 4. Minimum Solder Volume Termination Model

The geometry of the soldered terminations with minimum solder volume have been simplified as triangles at the sides (V_1, V_2) and end of the terminal contact (V_3) while the largest volume contributor to the solder joint is the rectangular area underneath it (V_4). The solder thickness dimension G contributes substantially to the overall solder joint volume. As the objective here is to determine a minimum solder volume, our interpretation of the 601E standard does not require the pad to be fully wetted to form an acceptable solder joint shape. The quantitative breakdown of this solder joint model is provided in Table 2. An acceptable ratio of solder paste to metal by volume is 2:1[6]. From this it is found that each chip component termination should require at least 0.48 nanoliters (1nl = 1,000,000µm^3) of printed solder paste volume to form an acceptable reflowed solder joint. Note this amount scales to the pad dimensions selected; i.e. smaller pads will not require as much solder paste to comply.

Table 2. Minimum Termination Solder Volume Result

	Solid Vol. (S) / Paste Vol. (2S)
$V_1 + V_2 = D \times F \times U =$	32200µm^3 / 64400µm^3
$V_3 = 0.5 \times F \times W \times Y =$	76763µm^3 / 153526µm^3
$V_4 = D \times G \times W =$	131250µm^3 / 262500µm^3
$V_{Total} = V_1 + V_2 + V_3 + V_4 =$	240213µm^3 / 480426µm^3
	~ 0.48 nanoliter

The printing stencil must be designed with aperture opening dimensions that will allow solder paste transfer accomplishing at least 0.48nl per pad. The difficulty in achieving this relates to practical restrictions on stencil thickness. For the products likely to see earliest implementation of M0201s, common stencil thickness used today is 100µm. The inclusion of M0201 will compel the use of even thinner stencil foils in order to reduce the risk of producing insufficient volume paste deposits attributed to clogged apertures. It is well documented that print transfer efficiency (TE) of solder paste scales proportionally to stencil aperture area ratio [7]. Area ratio (AR) is defined as the aperture opening area divided by the aperture wall area.

AR values reducing further away from 0.6 will escalate average paste transfer loss while also increasing scatter in printed deposit size and shape. This principle is described in Figure 5 where the thicker stencil is less capable to transfer its full capacity of solder paste due to excessive adhesion on the aperture walls. Similarly, shrinking aperture opening size contributes significantly to degrading the resulting AR value. For our pad dimensions using a comparably sized aperture with a stencil thickness of 100µm the AR is < 0.35. This is a critically low AR and impractical to expect reasonable printing performance.

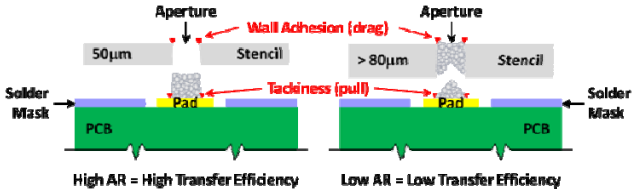


Figure 5. Stencil Aperture Size Influence on Paste Transfer

The decision was made to test the capability of printing M0201 pads through two different stencil thicknesses specified at 80µm and 50µm. Table 3 identifies the ARs corresponding to the different stencil thicknesses using a common rectangular aperture size designed to print nearly the full pad area. While the thinner stencil offers the larger AR and should permit more stable printing results, such a thin foil may not accommodate delivering the paste volume required to support coarser pitch standard component types. This point will be further explained in the stencil discussion section.

Table 3. Stencil Thickness, Aperture Size, and Area Ratio

Stencil Thickness (µm)	50µm	80µm
Aperture Size (µm)	120 x 140	120 x 140
Area Ratio	0.646	0.404

Given the minimum printed solder volume requirement of 0.48nl and comparing this to the proposed stencil aperture designs, we can now identify the print volume transfer efficiency levels necessary to accommodate. Figure 6 identifies the raw solder paste volume range for each stencil thickness that correlates against 25% through 100% transfer efficiency. The important point to note here is the position of the minimum required print volume of 0.48nl with respect to the printing capability of the two stencil designs. The volume transfer efficiency required to achieve this is 57% and 36% for 50µm and 80µm thick stencils respectively.

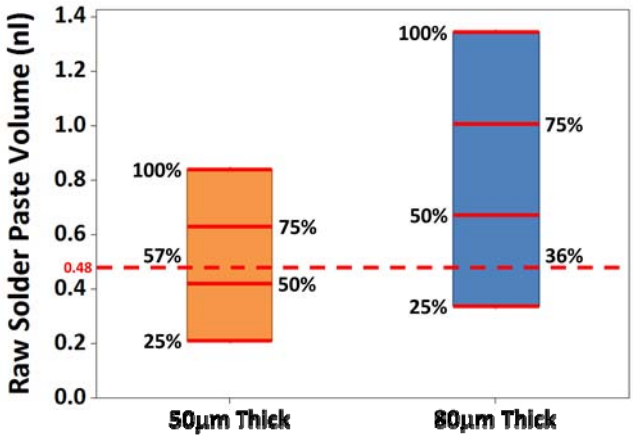


Figure 6. Solder Volume Transfer Efficiency Comparison

CIRCUIT BOARD

A printed circuit board (PCB) for the purpose of testing the assembly capability of M0201s was designed to represent a simulated 4-up mobile phone product. Other component footprint designs include 03015M passives, 0.3mm pitch chip scale packages, and a variety of other standard component types fit for such applications. This non-electrically functional test board is 150 x 100 x 1mm with Cu/OSP pads patterned on one side and Cu/OSP exposed surface on the opposite side. Figure 7a and Figure 8 refers. The M0201 land patterns are grouped inside each of the red circles in Figure 7a. Each circle contains 30 M0201 components, half of these positioned horizontally and half in vertical orientation (see Figure 7b).

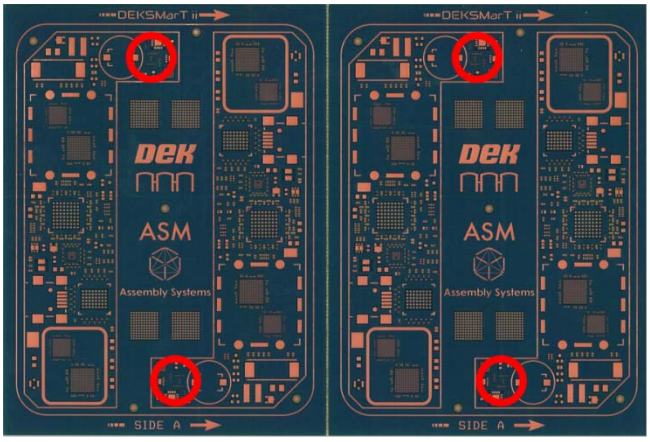


Figure 7a. Test PCB, Patterned Top Side (Side A)

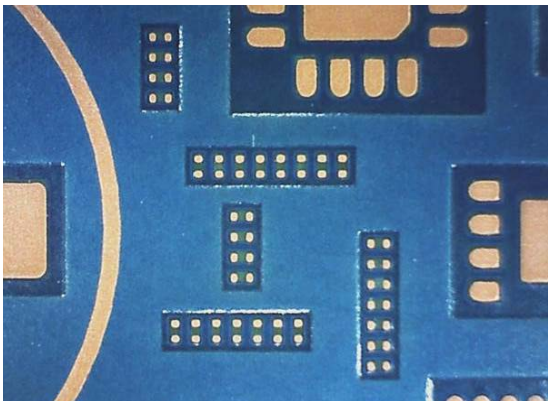


Figure 7b. M0201 Pads, 30 Component Group

Figure 8. Test PCB, Blank Bottom Side (Side B)

All M0201 pads were designed as non solder mask defined (NSMD) with a single solder mask opening area containing both pads. Given the small size of these pads it was expected that manufacturing this design would be difficult to control dimensional accuracy. Upon inspection of the boards we found all M0201s exhibited over-etched copper at various levels of severity. This observed discrepancy in Cu pad size has been carefully considered as a potentially significant variable of influence on resulting print performance. Several categories of board quality were identified with two groups designated of interest for further print process investigation. One board group consisted of full M0201 pads and the other group included only boards with significantly over-etched M0201 Cu pads. All boards in both groups comprised acceptable solder mask registration.

Example pad specimens from these board groups are shown in Figure 9. The boards exhibiting the fullest pads were still quite rounded in the corners, decreasing the copper land area by about 10% compared to the gerber (GBX) design. The small copper pads in comparison were over-etched by more than 80% in some instances. As shown in Figure 9, both large and small pad examples have significantly reduced solder mask window openings compared to the original GBX artwork. This attribute affects all boards.

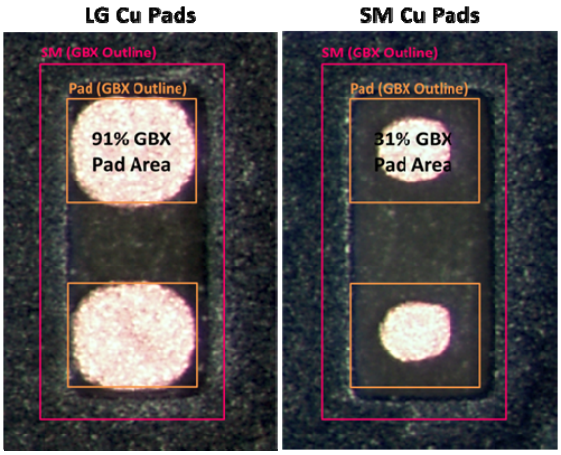


Figure 9. Variable M0201 Pad Quality Results

STENCIL

Stencil thicknesses of 50µm and 80µm were selected to study M0201 printing performance. While the thinner stencil should facilitate easier paste transfer, the 50µm thick stencil is not likely to permit printing enough solder paste volume for the majority of components designed on the test board. A printing challenge facing M0201 implementation is the reality that uniform thickness stencil solutions cannot be so thin. Selective stencil thinning, or step stencil designs, offer a compromise to use two different foil thicknesses on one stencil. While step stencil technology has been available for a number of years, its utilization is typically reserved for extenuating circumstances such as this where a significant component level discrepancy in solder volume demand exists. The stencil design we have features locally stepped regions on two of the four M0201 component groups, as indicated in Figure 10, where the top of the stencil has been chemically etched to reduce foil thickness from 80µm to 50µm.

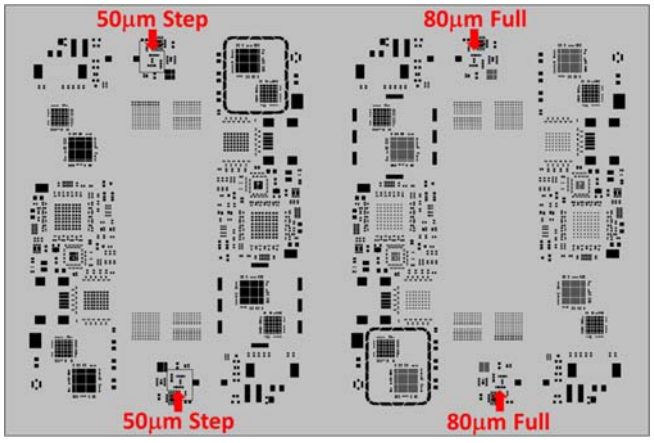


Figure 10. Stencil Artwork GBX Drawing

A detailed view of the step area shown in Figure 11 captures the arrangement of the M0201 apertures. The vast majority of PCB designs, including this one, are not configured optimally for step stencil printing. Ideally the step perimeter is rectangular and there is sufficient clearance or “keep out”

space between the apertures inset the step and the step border. The dimensions labeled in red color indicate the step border is too close to the aperture according to IPC policy illustrated in Figure 12 [7]. The "K1" (i.e. "keep out") zone should be > 1.08mm. Four of the six step wall perimeters violate the K1 rule. The main reason to accommodate the K1 margin is to permit enough space for a rigid squeegee to flex down into the step area and wipe the aperture top side surface clean. Any solder paste film or residue remaining on the stencil surface around aperture openings after the print stroke will destabilize transfer efficiency performance.

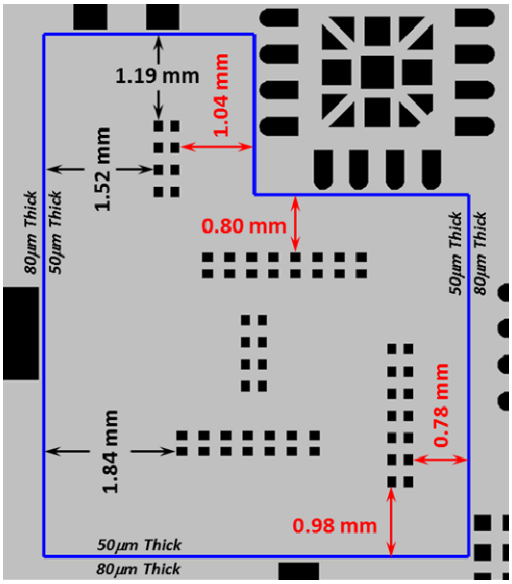


Figure 11. M0201 Step Area Borders & Violations

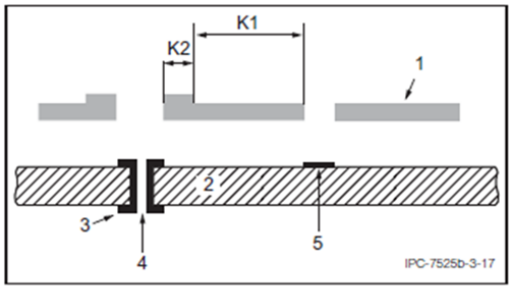


Figure 3-17 Overprint With Step (Squeegee Side)
1. Step Stencil 3. Through-Hole Land 5. SMT Land
2. Board 4. Through-Hole

Figure 12. Step Stencil Guidelines, IPC-7525B [6]

Two identical laser cut, 80µm base thickness, stainless steel stencils were manufactured. Both were step etched locally to 50µm as per the previous discussion. The type of stencils made were mesh-less format foils, whereby the metal sheet comprises nearly the entire stencil area and is fitted into a 23-inch square master frame which mechanically clamps and tensions the foil. The only difference between the two stencils is that one was produced with a polymer type nano-coating applied to its bottom side and the other stencil did not have any nano-coating.

Printing performance reports based on stencil nano-coatings have been a popular publication topic in recent years [8, 9, 10, 11, 12]. As the name implies, a nano-coating is a very thinly applied material adhering to the bottom side of a metal stencil containing flux repelling properties (i.e. fluxophobicity). The original function of a nano-coating was to assist in preserving the cleanliness of the stencil bottom side by preventing premature flux and solder particle smearing. There are also claims for nano-coated stencils to deliver higher print transfer efficiency enabled by reducing the adhesion and friction of paste on aperture walls.

A sample of 16 apertures from each stencil were manually measured using a coordinate measuring machine tool. Top and bottom side stencil foil measurements were compared for the same apertures in order to determine average dimensions. Comparing averaged aperture size of aggregated measurements for each stencil against the GBX designed aperture size, it was verified the stencils were manufactured within 4.5µm of specification.

PRINT TEST PREPARATION

The list of resources used to complete the M0201 print testing is supplied in Table 4. We decided to implement a printing process that included the most advanced and enhanced setup in order to create the best possible opportunity to print well. The printing machine used was a modern, well maintained, fully automatic, option loaded, state of the art model. Three key options on this machine that were used include automatic height adjusting edge snugging clamps, dedicated vacuum tooling, and ultrasonic squeegee technology. The virtues of these options have been previously reported [13, 14]. A Type 5 fine powder solder paste material recommended for miniature device printing was used exclusively. As previously described, one laser cut stencil was treated with a polymer nano-coating, otherwise the two stencils are identical.

Table 4. Experiment Tools, Materials, & Settings

Printer	ASM DEK Horizon01iX
Clamps	Over Top Snugger
Tooling	Dedicated Vacuum Block
PCBs, Print Order	Number labeled boards
PCB Print Side	Side A Pads, Side B Blank
Solder Paste	Indium 8.9HFA, SAC305, NC, 88.75%, Type 5
Stencil Frame	Vector Guard 260 (23"x23")
Stencil Thickness	Step - 50µm, Full - 80µm
Nano-Coating	Sten. 1 - Nano-Coated, Sten. 2 Un-coated
USC	Under Stencil Cleaner not used
Print Speed	50mm/sec
Print Pressure	4.6kg
Separation Speed	1.0 mm/sec
Separation Distance	3.0 mm
Print Procedure	2 Dummy + 10 Meas. Prints, Uninterrupted
Print 1 Direction	Reverse
Squeegees	ProActiv Squeegee, 170mm blade
SPI Machine	Koh Young 8030-3, 10µm Camera

The printing procedure consisted of using fixed process parameters of conservative, but practical levels that should accommodate mass printing tempo. In order to view the natural degradation of the printing process the automatic under stencil wiping process was disabled. Each print test run consisted of two warm-up prints on blank boards, followed by ten consecutive test prints that were subsequently measured by advanced SPI equipment.

Table 5 denotes the experiment variable list and run order. Three categories of PCB include printing on the Bare Cu backside of the board, Large Pad sorted boards, and Small Pad sorted boards. The stencil aperture is considered to have the best gasketing opportunity for printing on the Bare Cu side, while having the worst gasketing opportunity printing on the Small Pads. The first three print tests involved the three different board types and were all printed using the nano-coated stencil. The remaining three print tests repeated the same process, except using the un-coated stencil. Print Test 7 was added in order to validate the results from Test 4.

Table 5. Experiment Variables, Run Order

	Nano-Coated	Un-Coated
Bare Cu (Side B)	Test 1	Test 6
Large Pad (Side A)	Test 2	Test 5
Small Pad (Side A)	Test 3	Tests 4, 7

RESULTS

The data from the complete printing experiment outlined in Table 5 is consolidated into a single interaction plot comparing mean paste volume transfer efficiency results in Figure 13. The values in Table 6 report the specific data plotted. Data labels ❹ and ❼ identify repeat Test 4 and Test 7 results. The plotted point in-between indicates the average of the two test conditions. Test 4 and 7 results are more alike to one another for the 50µm thick step stencil apertures due to a more favorable area ratio permitting easier paste transfer compared to the full 80µm thick stencil apertures. The red horizontal dashed line highlights the 70% paste transfer efficiency threshold which is a common transfer efficiency target for standard printing applications. The data is quite distinctively divided above and below this threshold, with the all the 50µm thick step stencil apertures performing at or above 100% average TE and all the full 80µm thick stencil apertures performing at or below 70% average TE. This divided pattern supports area ratio logic.

Further interrogation of the data shows the Bare Cu printed boards to yield lower paste transfer than the NSMD Cu pads in 3 of 4 instances. The PCB topography introduced by solder mask openings and patterned metallization leads to improper stencil gasketing during the aperture fill process, likely allowing the additional paste volume to be deposited. For both LG and SM Cu pads, the nano-coated stencil results in overall solder paste transfer efficiency improvement compared to the un-coated stencil. The only condition where stencil nano-coating has a negative influence on average paste transfer is for the full 80µm thick stencil apertures printed on Bare Cu. Reference [10] also reports average volume paste transfer efficiency data where the nano-coated stencil produces less paste volume (compared to an un-coated stencil). It is explained in [10] that the nano-coating assists to improve the shape of the print deposits to more closely resemble the true form of the stencil aperture. In contrast, the un-coated stencil may produce printed deposits that exhibit some shape distortion that contributes to inflated transfer efficiency values.

Table 6. M0201 Mean Paste Volume Data

	50µm Thick Stencil		80µm Thick Stencil	
	Nano-Coated	Un-Coated	Nano-Coated	Un-coated
Bare Cu (Side B)	102%	98%	56%	60%
Large Pad (Side A)	125%	109%	69%	61%
Small Pad (Side A)	124%	116%, 114%	71%	53%, 65%

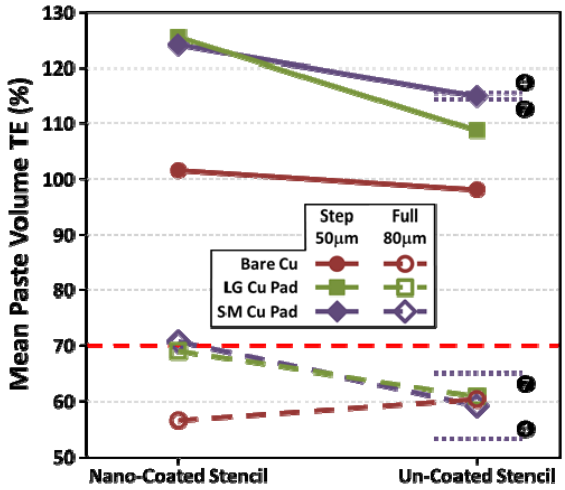


Figure 13. M0201 Mean Paste Volume Trends

While the logic for improved solder paste deposit shape ascribed to a stencil nano-coating seems reasonable, this does not make complete sense upon considering the standard deviation data. The same 80µm thick stencil aperture print results on Bare Cu boards exhibits a contradicting trend as shown in the standard deviation interaction plot of Figure 14. The values in Table 7 report the specific data plotted. An improved solder print deposit shape should also correlate to better uniformity marked by reduced standard deviation value, which in fact has not occurred for the nano-coated stencil result. Our explanation for this reduced printing capability is the discovery of a unique set of conditions for which the function of a stencil nano-coating hinders printing performance. Such conditions are now thought to consist of a stencil nano-coating in combination with challenging aperture area ratio designs while printing onto a flat surface where the stencil gasket condition is ideal. Additional validation testing is required to grow confidence in this fresh hypothesis.

Further review of Figure 14 show the nano-coated stencil apertures improved standard deviation for all test conditions except for the 80µm stencil apertures printing on Bare Cu.

The effect of nano-coating apertures appears to have the greatest performance benefit for the SM Cu pads, improving standard deviation by at least 10%. Also in 3 of 4 cases, the SM Pad print uniformity is worse than the LG Pad result, despite showing nearly equal average TE values. The main reason for replicating Test 4 (❹) with Test 7 (❼) was to confirm the occurrence of large standard deviation and significantly insufficient deposits to be reproducible. This was indeed proven. Another feature of the graph is the red dashed horizontal line indicating the 10% standard deviation level which marks a common threshold identifying print process control. Values above this typically indicate undesirable printing deposit uniformity, which is the case for nearly all our data. The most controlled print volume distributions result from printing on the Bare Cu, i.e. smoothest surface. It is somewhat unexpected to see the higher area ratio apertures designed on the thinner 50µm step stencil producing consistently higher print deposit scatter compared to the low area ratio stencil apertures on the thicker 80µm foil. The explanation for this is the inability for the squeegee blade to effectively wipe the solder paste cleanly inside the step pocket area. As previously indicated in Figure 11 the step size and geometry is not optimal. A favorable aperture area ratio design is not enough compensate for a poor stencil wipe.

Table 7. M0201 Paste Volume Standard Deviation Data

	50µm Thick Stencil		80µm Thick Stencil	
	Nano-Coated	Un-Coated	Nano-Coated	Un-coated
Bare Cu (Side B)	9%	11%	12%	10%
Large Pad (Side A)	20%	28%	15%	17%
Small Pad (Side A)	24%	35%, 35%	12%	26%, 22%

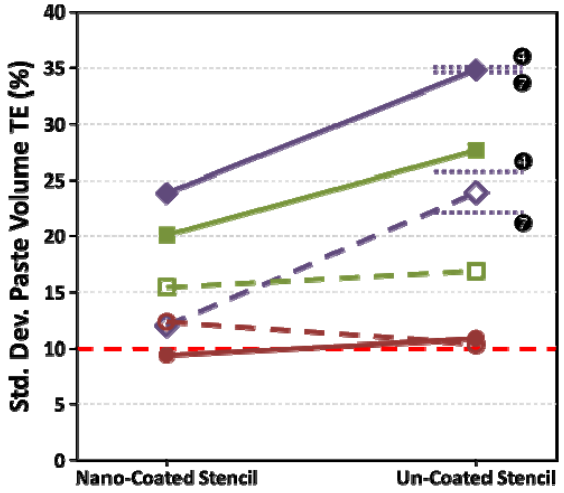


Figure 14. M0201 Paste Volume Standard Deviations (same legend applies from Figure 13)

Another view of the M0201 data considers the raw print volume distribution results in the boxplots on Figure 15. It was earlier described in Figure 4 a model for estimating the lowest solder volume accomplishing an acceptable soldered termination result. The result in Table 2 indicates a raw print volume of 0.48nl satisfies this requirement and is identified in Figure 13 as the dashed horizontal red line. It is useful to view this threshold against the raw solder paste print data to improve judgment on M0201 printability. The only test condition which supplied enough solder paste on all ten prints is the 50µm thick step stencil nano-coated apertures. This result may actually be enabled by a poor stencil wipe as the side effect of this can be additional paste volume, confirmed by the high TE reported in Figure 13. Another interesting general observation here is the similarity of raw print volume distributions when comparing the 50µm thick step stencil data against the full 80µm thick stencil. While we may expect to see more physical paste volume delivered by the thicker foil, the trend in fact is just the opposite with the thinner foil supplying more volume. Reasoning for this is the combination of a more challenging area ratio on the 80µm thick stencil that limits paste transfer efficiency along with the poor stencil wipe condition inside the 50µm thick step areas which boosts print volume. Further review of Figure 15 results show there are a few test conditions that nearly satisfy the minimum 0.48nl paste volume requirement. The data distributions can be dissected in more detail by exploring the raw print volume distributions on an individual print basis, which is explored in Figures 16, 17, and 18.

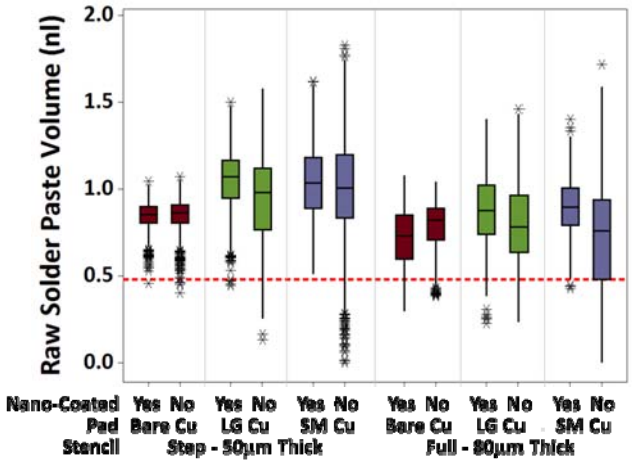


Figure 15. Raw Volume Boxplot - All Prints Combined

While the format of the boxplots in Figures 16, 17, 18 are labeled for clear interpretation, two key performance metrics necessitate clarification. First, the 0.48nl paste volume threshold is drawn in these plots now as a blue colored dashed horizontal line. Second, the outline color of the individual boxplot is either red or black. Red boxplot outlines indicate the print volume distribution exceeds a volume transfer efficiency standard deviation value of 10%. Black boxplot outlines indicate the standard deviation is less than 10%. The objective for investigating these detailed boxplot views is to determine which data, if any, is able to satisfy both conditions (i.e. > 0.48nl, < 10% Std. Dev.) Figure 16 contains several occurrences of compliant data, representing the printing process test on Bare Cu boards. The flatter board topography is considered a significant advantage towards achieving highly uniform prints. Despite

the challenge of efficient squeegee wiping inside the 50µm thick step area, several boards were printed quite well. Fewer successes were reported with the thicker 80µm apertures, as expected with lower area ratio apertures.

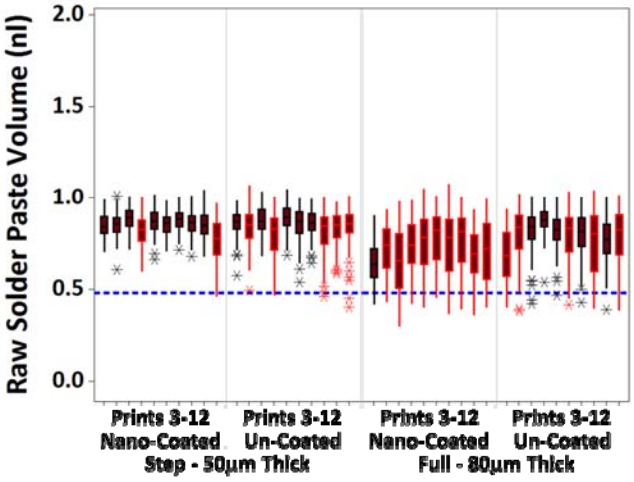


Figure 16. Individual Print Boxplots - Bare Cu Pads

The print by print results in Figure 17 contains LG Pad data. Some of the boards printed with nano-coated stencil apertures satisfy the 0.48nl paste volume requirement, however, none of the prints demonstrate less than 10% standard deviation.

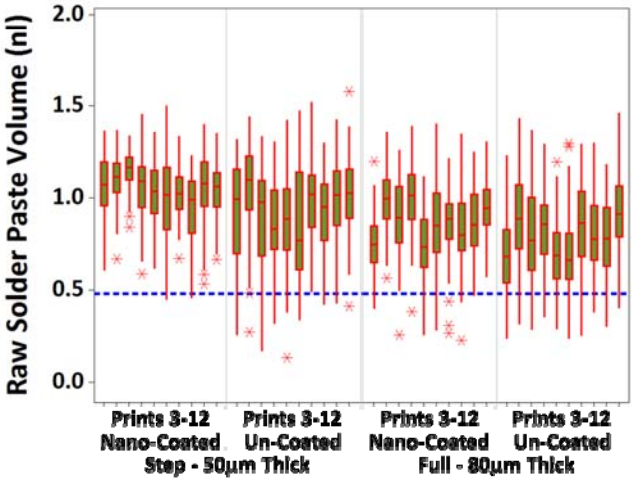


Figure 17. Individual Print Boxplots - Large Cu Pads

The print by print results in Figure 18 contains SM Pad data. Only one in 40 boards satisfies the 0.48nl paste volume and 10% standard deviation criteria. The benefit of the stencil nano-coating is particularly obvious for this data set as an extreme number of low volume outliers occur on boards printed with the un-coated stencil.

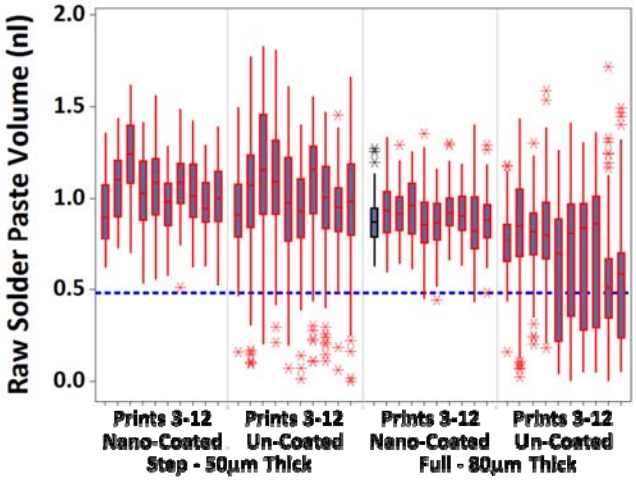


Figure 18. Individual Print Boxplots - Small Cu Pads

CONCLUSION

The results of this printing research largely support the printing capability benefits offered by using nano-coated stencils. The largest benefit observed from the nano-coating was reduced print volume distribution scatter, particularly on the circuit boards with small undersized Cu pads. The discovery of one unique test condition combination that produced poorer printing performance with the nano-coated stencil is currently unexplainable and warrants further review to confirm consistency of this behavior.

This work has also identified the effect of pad structure to have profound influence on printing results, with the planar Bare Cu board surface performing stand-alone best. However, demonstrated printing capability on bare board surfaces does not guarantee the same success on real patterned PCBs. Board design and manufacturing quality can significantly influence the printing outcome. While average print volume transfer efficiency results were similar comparing large pads against small pads, the print volume uniformity was noted better on large pads.

M0201 printing capability on proper circuit board pads proved to be best controlled using the 80µm thick nano-coated stencil despite the unfavorable area ratio compared to the 50µm thick step stencil results. The 50µm thick step stencil apertures printed much larger than expected paste volume and produced a wider scatter in the print volume distribution attributed to poor squeegee wipe efficiency inside the step area.

FURTHER WORK

Work will continue to improve print quality results on both 80µm thick and 50µm thick stencil foils on this test board. A subsequent M0201 full assembly and reflow experiment is currently in plan.

REFERENCES

[1] M. Whitmore, J. Schake, C. Ashmore, "Factors Affecting Stencil Aperture Design For Next Generation Ultra Fine Pitch Printing", Proceedings of SMTA International Conference on Soldering and Reliability, May 2013.

[2] Murata Manufacturing Co., Ltd., "GRM01121C1E100JE01 (008004, CH, 10pF, DC25V)", Reference Sheet, p.1.

[3] http://www.marketwatch.com/story/muratas-worlds-smallest-008004-size-025-x-0125-mm-chip-ferrite-bead-2013-09-24

[4] Murata Manufacturing Co., Ltd., "GRM01121C1E100JE01 (008004, CH, 10pF, DC25V)", Reference Sheet, p.25.

[5] Product Assurance Committee Task Group 7-31b, "Acceptability of Electronic Assemblies", IPC-A-610E, April 2010.

[6] J. Schake, M. Whitmore, "Stencil Printing Solder Paste and Transfer Efficiency - Establishing the Baseline", Proceedings of SMTA International, September 2004.

[7] Stencil Design Task Group 5-21e, "Stencil Design Guidelines", IPC-7525B, October 2011.

[8] M, Rösch, J. Franke, C. Läntzsch, "Characteristics and Potentials of Nano-Coated Stencils for Stencil Printing Optimization, Proceedings of SMTA International, October 2010.

[9] M. Kelly, W. Green, M. Cole, R. Kellmann, "Plasma Stencil Treatments: A Statistical Evaluation", Proceedings of SMTA International, October 2013.

[10] C. Shea, M. Bixenman, D. Carboni, B. Sandy-Smith, G. Wade, R. Whittier, J. Perault, E. Hansen, "Quantifying the Improvements in the Solder Paste Printing Process from Stencil Nanocoatings and Engineered Under Wipe Solvents", Proceedings of SMTA International Conference on Soldering and Reliability, May 2014.

[11] T. Lentz, "Performance Enhancing Nano-Coatings: Changing The Rules of Stencil Design", Proceedings of SMTA International, September 2014.

[12] C Salewski, J. L'Heureux, "Highly Accurate 3D Solder Paste Inspection Comparing Nano Coated Stencils with Non-Coated Results", Proceedings of SMTA International, September 2014.

[13] J. Schake, M. Whitmore, C. Ashmore, "Stencil Aperture Design Considerations for 0.3 CSP Ultra-Fine Pitch Printing", Proceedings of SMTA International, October 2013.

[14] M. Whitmore, C. Ashmore, "The Next Big Challenge for Stencil Printing – Sub 0.5 Area Ratio Apertures", Proceedings of SMTA International, September 2014.