FEA AND ANALYSIS FOR BGA/CGA ASSEMBLIES UNDER THERMAL CYCLING

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ABSTRACT

Even though commercial off the shelf (COTS) column grid arrays (CGAs) have been widely used in high-reliability electronics-system applications, the ball grid array (BGA) versions are also becoming attractive because of newer technology availability, much lower cost, and lower CTE mismatches onto polymeric printed circuit boards (PCBs). For these reasons, and because of availability of extensive reliability data, university and industry sectors have developed and now offer software for projecting solder joint reliability for BGA assemblies subjected to thermal cycling conditions.

A commercial software recently developed was evaluated to determine its accuracy in projecting solder joint reliability comparing test data for BGAs and land grid arrays (LGAs) with 1156 balls/terminations. In addition, two dimensional finite element analyses (FEAs) were carried out to determine stress distribution for the LGA/BGA as well as for a CGA with 1272 columns. Only the FEA analysis was presented for CGA since the commercial software does not yet offer projection for this packaging style. Finally, this paper summarizes these findings and presents an easy to use analytical model developed to predict the behavior of BGA and CGA assemblies under thermal cycling conditions.

Key words: Solder joint reliability analysis, ball grid array, land grid array, column grid array,thermal, solder joint reliability, BGA, LGA, CGA, CCGA

INTRODUCTION

This paper focuses on the second-level (board-level) solder joint reliability modeling, projection, and comparison of test data for ball grid array (BGA), land grid array (LGA), and ceramic column grid array (CGA). Industry has a wealth of publication on the 2nd level assembly reliability of BGA categories, but a co-author has published extensively on CGAs as well as BGAs within the last two decades [1-12].
Figure 1 categorizes single-chip microelectronics packaging technologies into three key technologies:

- Plastic ball grid arrays (PBGAs) including flip-chip die version (FCBGA), land grid array (LGA) with solder balls, quad flat no lead (QFN) and new versions
- Ceramic ball grid array (CBGA), ceramic column grid arrays (CGAs), and ceramic LGA version
- Chip-scale packages, a smaller foot print versions of BGA and wafer level packages (WLPs.)

PBGAs and CSPs are now widely used for many commercial electronics applications, including portable and telecommunication products. BGAs with 0.8-1.27-mm pitches are implemented for high reliability applications, generally demanding more stringent thermal and mechanical cycling requirements. The plastic BGAs were introduced in the late 1980s and implemented with great caution in the early 1990s, and further evolved in the mid-1990s into the CSP (also known as a fine-pitch BGA) having a much finer pitch from 0.4 mm down to 0.3 mm. Recently, fan-out and fan-in wafer level packages have gained significant interest.

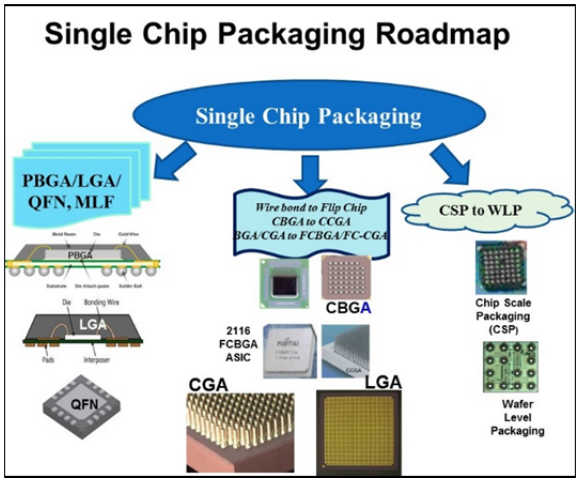

Figure 1. Single chip packaging technologies covers three main categories.

Solder joints are the key interface element for BGA/LGA/CGA packages on to PCBs (assemblies). Reliability under thermal stress for packages and assemblies depend on the reliability of constituent elements and global/local interfaces [13, 14]. Solder joints in BGA/CGA are unique since they provide both electrical interconnection and mechanical load-bearing elements for the attachment of a package onto a PCB and often function as a critical heat conduit too. A solder joint in isolation is neither reliable nor unreliable; reliability has meaning only in the context of interconnections either within a package or outside of a package onto PCB. For BGA/CGA package assembly, it is critical to also determine the key parameters affecting assembly reliability under thermal, mechanical, and combination loadings.

Under thermal loading, the CGA assembly elements that play key roles in defining reliability are affected by the

global and local coefficient of thermal mismatches (CTEs) and solder alloy properties as schematically shown in Figure 2. The characteristics of three elements — package (e.g., die, substrate, solder joint, underfill), PCB (e.g., polymer, copper, plated through hole, microvia), solder joints (e.g., via balls, columns) — together with the use conditions, the design life, and acceptance failure probability for the electronic assembly determine the reliability of CGA assemblies. In addition, for CGA, solder columns also act as a load carrying element between a package and a board similar to metallic leads such as those for a CQFP. Column flexibility and length to diameter ratio affect load bearing capability and are considered in the analyses.

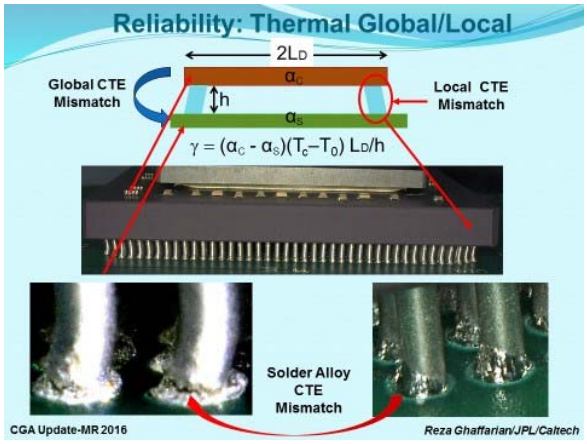

Figure 2. Three key elements that define reliability under thermal stress are due to the global, local, and solder alloy coefficient of thermal (CTE) mismatches.

The global expansion mismatches result from differential thermal expansions of a package and the PCB assembly. These thermal expansion differences (Δ) stem from differences in the coefficient of thermal expansions (CTEs) and thermal gradients as the result of heat dissipation from functional die within package. Global CTE-mismatches typically range from □α~2 ppm/°C ($2x10^{-6}$) for CTE-tailored high reliability assemblies to □α ~14 ppm/°C for ceramic packages (e.g., CGA) on an FR-4 PCB. The thermal expansion mismatch representative of the global CTE mismatch due to thermal excursion is given as the following.

$$\Delta = (\alpha_C - \alpha_S)(T_c - T_0) L_D = (\Delta\alpha)(\Delta T) l \qquad (1)$$

Global CTE mismatches are typically the largest, since all three parameters determining the thermal expansion mismatches are large: the CTE-mismatch (Δα), the temperature swing (ΔT), and the distance to neutral point (DNP) (half of the largest acting package diagonal length (l or L_D)). Shear strain ($\Delta\gamma$) is directly proportional Δ , but inversely proportional to solder joint height, h_s as shown in relationship in Eq. 2.

$$\Delta\gamma = C\frac{L_D}{h_s}\Delta\alpha\Delta T \qquad (2)$$

Solder Joint Reliability Modeling Methods

Significant work has been devoted for life prediction and reliability of solder joints for conventional and advanced electronics packaging at the assembly level. In the past, the life projection methodology focused on using a modified version of the Coffin-Manson empirical model, e.g., Engelmaier [13, 14], based on correlation with limited test data. Therefore, as more data on the same technology, or data for newer technologies become available, these models were continuously updated with inclusion of new parameters. For example, Chauhan, e al. discuss on the expansion of deficiency of this model and expansion with new parameters for both tin-lead and lead-free solder alloys. Other newer models proposed includes crack propagation and strain energy accumulation approaches that are also had been used to fit experimental test data both for tin-lead and lead-free solder joint attachment.

Wong et al., [16] state that the goal of creep fatigue modelling is to determine the compounding effects of damage caused by creep and fatigue mechanisms, but modelers have disregarded aspects of these damages. Literature survey shows that modelers: (1) have ignored fatigue damage and used only creep ductility, (2) have combined creep and plastic strain/energy even though they are different, (3) have performed linear summation of fractional creep and fatigue damage, (4) have partitioned damage into creep, fatigue, and interaction followed by linear summation of fractional damage, (5) have used a common parameter to model creep and fatigue damage, (6) have used a separate damage parameter to model creep and fatigue damage, and (7) have integrated creep functions into fatigue equation known as creep-modified fatigue. In conclusion, a good model should capture damages from both pure creep and fatigue— the Engelmaier relationship does not, whereas unified equation does.

The Coffin-Manson empirical relationship which was developed in early 1950's is commonly used for fatigue life prediction (cycle-to-failure, N_f). Engelmaier has proposed modified versions of the Coffin-Manson model [13, 14] for package thermal cycle life calculation. For stiff leadless SM solder attachments, for which the stresses in the solder joints exceed the solder yield strength, the predictive equation for thermal cyclic loading is:

$$N_f(x\%) = \frac{1}{2}\left[\frac{2\varepsilon_f'}{F}\frac{h}{L_D\Delta\alpha\Delta T_c}\right]^{-1/c}\cdot\left[\frac{\ln(1-0.01x)}{\ln(0.5)}\right]^{1/\beta} \qquad (3)$$

The "F" value is continuously updated and, for example, it states that for metric units, the scaling coefficient "F" is 1.38 MPa (instead of 200 Ibf/in2), and for near-eutectic tin/lead (63/37 and 60/40) solders. For other solders including SAC, the coefficients are expected to have different values including the creep/fatigue exponent c. For tin-lead c is given as

$$c = -0.442 - 6\times10^{4}\overline{T_{SJ}} + 1.74\times10^{-2}\ln\left(1+\frac{360}{t_D}\right) \qquad (4)$$

Various versions with different parameters of the above relationship; which is based on strain range, have been considered by university and industry to project cycles to failure. For example, in a university software model [15], fatigue life is calculated as a function of strain range and this model provides a new fatigue exponent ductility constant specific to solder types including tin-lead and lead-free solder assemblies. Unfortunately, we were unable to access this software in time to provide a comparison with the commercial software since this software is only available to the university's consortium members.

We were licensed to use a commercially available software for solder joint-reliability projection. This newly developed software [17, 18] combines a number of relationships to project cycles to failure: (1) strain range from the Engelmaier relationship [13, 14], (2) stress from force balance between package and PCB, and (3) cycles to failure projections from relationship to strain energy (stress times strain). Equation 5 is used for shear stress, which is calculated by using the force balance equation and comparing the amount of displacement due to thermal cycling and mechanical loading induced on solder. Equation 6 is used to determine strain energy density (ΔW), it is calculated by multiplying shear stress and strain range. Based on the energy density, fatigue life is calculated using the energy based fatigue equation developed by A. Syed [19] for tin-lead (equation 7) and SAC lead-free (equation 8).

$$(\alpha_2-\alpha_1)\cdot\Delta T\cdot L_D = F\cdot\left(\frac{L_D}{E_1A_1}+\frac{L_D}{E_2A_2}+\frac{h_s}{A_sG_s}+\frac{h_c}{A_cG_c}+\left(\frac{2-\nu}{9\cdot G_b a}\right)\right) \quad (5)$$

$$\Delta W = 0.5\cdot\Delta\gamma\cdot\frac{F}{A_s} \quad (6)$$

SnPb $$N_f = \left(0.0006061\cdot\Delta W\right)^{-1} \quad (7)$$

SAC $$N_f = \left(0.0019\cdot\Delta W\right)^{-1} \quad (8)$$

Suhir, et al. [20, 21]) presented another simple and easy to use analytical approach using various solid mechanics methods to determine stress and strain equations for BGA/CGA assemblies under thermal stresses. Use of the tri-materials stress analysis method allows the comparison of the effect of double-sided assembly with a mirror-image configuration. Many aspects of BGA/CGA assemblies under thermal stresses were discussed. One aspect was to answer the question if application of CGA results in inelastic-strain free in solder materials, if so, then, , high-cycle fatigue failure behavior become dominant rather than low-cycle fatigue failure with plastic deformation. The model assumes use of a short cylinder, a beam representing of a column in CGA, that is subjected to bending deformation. The beam's ends are considered to be clamped and offset. The offset in CGA (Δ) is estimated from the thermal-mismatch strain between the CGA and the PCB for a given joint as function of its DNP. The analyses are limited to elastic deformation only.

The following formulas (equations 9 and 10) are derived for the maximum shear and normal stresses by assuming a short cylinder (beam) of diameter d and height h (length). Beam's flat ends are clamped and offset at the given distance of Δ.

$$\tau_{\max} = \frac{9}{8}E\frac{\Delta}{d}\left(\frac{d}{h}\right)^3\left[1+\frac{27}{10}(1+\nu)\left(\frac{d}{h}\right)^2\right], \quad (9)$$

$$\sigma_{\max} = 3E\frac{\Delta}{d}\left(\frac{d}{h}\right)^2\left[1+\frac{27}{10}(1+\nu)\left(\frac{d}{h}\right)^2\right] = \frac{8}{3}\frac{h}{d}\tau_{\max}. \quad (10)$$

Here ν , is Poisson's ratio of the material.

These equations indicate that for a beam analysis, the normal bending stress always exceeds the shearing stress (8/3 (h/d) >1 since h>d). For the height/diameter (h/d) ratio of above 12-15, these relationships confirm the well-known condition that the shear stress does not have to be accounted for. This statement is true whether one uses the classical Timoshenko model— the displacement of a cantilever beam subjected to a force applied to the beam's end— or uses this analysis when the maximum force and the corresponding stresses are given as an ends' offset. The stress analyses were expanded to determine thermally induced stresses in BGA and CGA assemblies using three steps.

First, the effective interfacial shearing and peeling stresses, as well as the corresponding displacements, were determined with the assumption that no inelastic stresses and strains take place. Next, stresses and strains for peripheral joints were evaluated from the first step values of in-plane (shearing) and through-the-thickness displacements. These displacements consider the role of the compliance of the assembly components and the joints themselves at the joints' ends.

This approach allows the boundary conditions to be somewhat different from the simple clamped-clamped conditions. For this case, then, the offset of the joint ends might be different than the one computed as the product of the thermal expansion mismatch strain $\Delta\alpha\Delta t$ and DNP. If the calculation showed elastic behavior condition, then, no need for continuation to the third step calculation. However, if the stresses exceeds the yield stress of the solder material, then the inelastic strain zone should evaluated at the third step. The inelastic values are then calculated by assuming that the solder material behaves linearly elastic below the yield strain and ideally plastic above the yield strain. Clearly, if the actual solder material exhibits elasto-plastic behavior above the yield strain, the corresponding states of stress and strain are between the extreme cases of the linearly-elastic and ideally plastic solutions. The methodology for BGA/CGA was further extended for estimating the effect of double-sided mirror-image assemblies.

THERMAL CYCLE TEST RESULTS

Test Vehicle and TC results for PBGA1156

The inputs of modeling parameters were measured from test vehicle build from LGA1156 and BGA 1156 that were assembled onto PCBs and subjected to thermal cycling to determine cycles to failure. For BGA1156, their assemblies showed low voids with no shorts or other anomalies were apparent based on X-ray evaluation and daisy-chin continuity measurements. Figure 3 shows a representative real time x-ray inspection revealing no signs of anomaly or damage. Generally, it is difficult to detect solder joint microcracks/damage by x-ray.

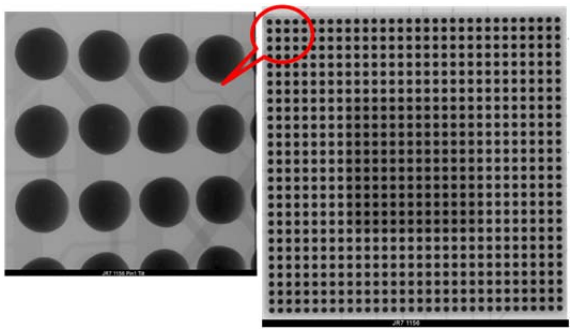

Figure 3. Representative X-ray photomicrograph for BGA 1156 I/O after assembly. Note the die is relatively small compared to the body size of the package

The assemblies were subject to three different thermal cycles (–55°/100°C –55° /125°C, –120°/ 85°C) and passed more than 200 cycles. After completion of further cycling, they were subjected to SEM and cross-sectional evaluations. Figure 4 shows representative SEM photomicrographs of the PBGA 1156 I/Os sample prior to x-sectioning diagonally through the center of the package in order to reveal the microstructure of internal interconnections. It specifically shows balls under the die that were expected to exhibit more severe stress conditions due to a larger thermal cycling coefficient-of-thermal-expansion (CTE) mismatch. Except for very fine microcracks at the package interfaces, no severe degradation was observed, either under the die or throughout the x-section (see Figure 5). Minor separation apparent at the die attachment may be either due to die bond separation or edge effects due to mounting of the sample and subsequent polishing.

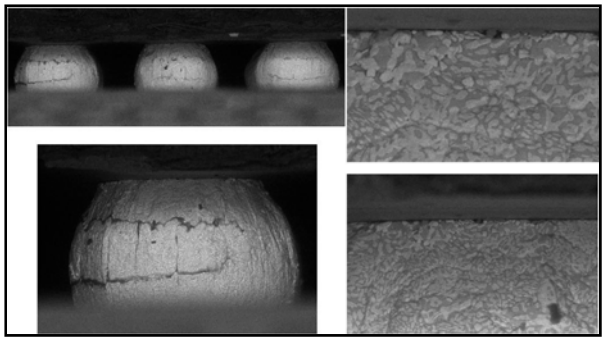

Figure 4. Representative SEM photomicrographs of a PBGA 1156 assembly after thermal cycling and prior to cross-sectioning.

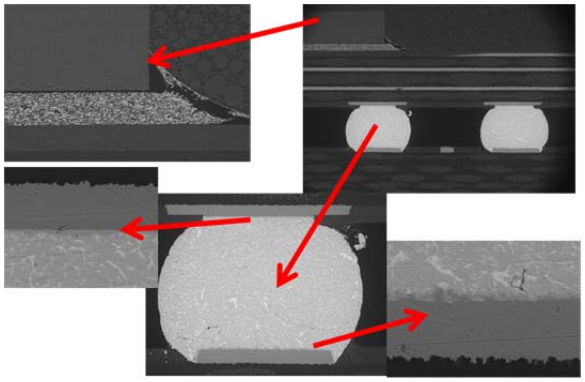

Figure 5. Cross-sectional SEM photomicrographs of PBGA 1156 I/Os assembly after thermal cycling.

TC Results for LGA1156

To determine the manufacturing challenges of LGAs and the effects of other packaging parameters, a new printed circuit board was designed to accommodate both high I/O ceramic and plastic LGA packages. The ceramic LGA had 1272 lands, whereas the plastic version had 1156 lands. All packages including LGAs had daisy-chain patterns for checking resistance continuity or opens after assembly and during reliability evaluation. High I/O LGA daisy-chain patterns not only enabled solder joint reliability evaluation, it also provided another verification method for the condition of interconnections after assembly. The PCB daisy-chain patterns were designed to match LGA designed packages such that a complete resistance loop was made after the package was assembled onto PCB. Three key parameters were evaluated before being ready to commit for a larger number of assemblies for reliability evaluation.

Generally, after LGA bake for moisture removal, tin-lead eutectic solder paste was applied on LGA pads and were reflowed to form solder domes on their pads. Ceramic packages are required to repeat the process in order to achieve desired height of solder dome. After the solder paste application on the PCB pads, the ceramic and the plastic LGAs are placed onto PCB and are prepared for assembly. No spacer shim was given for the plastic LGA, whereas a 5-mil spacer shim was used for ceramic LGAs in order to avoid the collapse of the package due to its heavy weight onto the board during reflow process. Figure 6 shows a

photo of the bumped plastic and ceramic LGAs (1156 and 1272 I/Os) and the final assembly. The test vehicle was assembled using a vapor- phase reflow machine. The Kapton tape was used as spacer for the ceramic LGA assembly is still apparent in the photo.

Real time 2D x-ray of the two package assemblies revealed no shorts or excessive solder balling and are considered to be acceptable. This build was repeated one more time achieving acceptable results. Figure 7 shows the overall X-ray of the side of LGA1156: it also shows the corner solder joints at a higher X-ray magnification. The X-ray shows the internal configuration of LGAs and fine pitch packages. During a real time review of the X-ray images at higher magnifications, no unusual solder anomalies were apparent, except some large voids.

Figure 6. HDI PCB with plastic and ceramic high I/O packages LGA assembly. Both plastic 1156 I/O (top left) and ceramic 1272 I/O LGAs had solder paste added and reflowed before assembly.

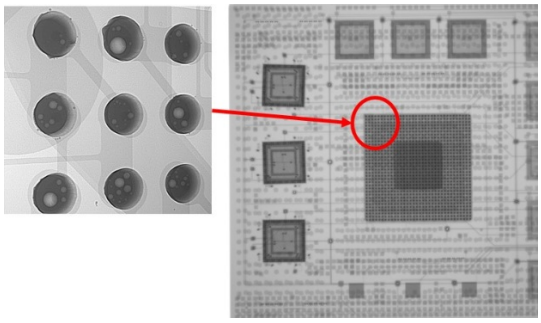

Figure. 7. X-ray photomicrographs of section of TV6 that includes plastic LGA1156 with solder joint voids.

TC Results for CGA1272

R. Ghaffarian presented his recent thermal cycle test data [22] for the CGA assembly under thermal cycling and drop followed by thermal cyclin. Only one relevant test data is summarized in this section. The CGA 1272 assemblies were subject to (-55/100°C) and another, more extreme cycle in the range of –55 to 125°C with a 2° to 5°C/min (3°C/min) heating/cooling rate. Visual inspection was performed to establish damage progression of outer columns of CGAs at thermal cycling intervals by optical microscopy. Figure 8 presents representative photomicrographs of solder-joint condition and damage progression due to thermal cycling in the range of –55 to 125°C at 500 cycles.

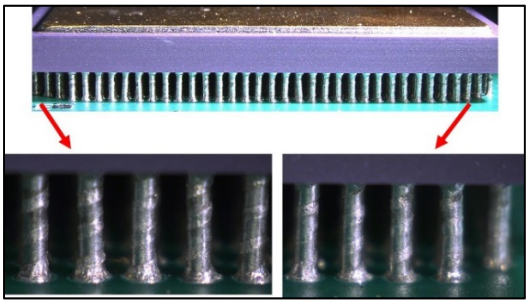

Figure 8. Representative photomicrographs of solder-joint quality after 500 thermal cycles (–55/125°C) for CGA1272.

MODELING OF LGA/BGA WITH 1156 LANDS/BALLS

LGA were assemblies subjected to two different thermal cycle and thermal shock cycle regimes, one was then cross-sectioned to determine solder joint integrity and the parameters needed for modeling. Figure 9 shows a cross-section of a LGA1156 with package dimensional values including die size/thickness, and solder joint height. These values are used for modeling both using commercial software and FEA.

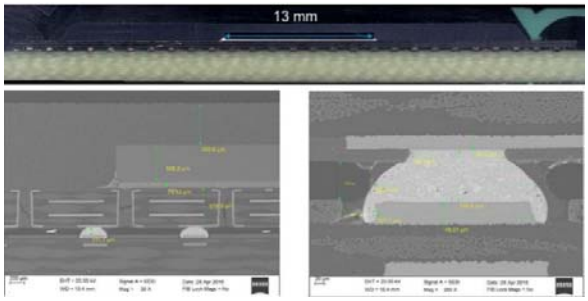

Figure 9. Representative photomicrographs of LGA1156 after thermal cycling with dimensional parameters for modeling.

Finite element Model design

The PBGA package, with 1156 area arrays with either solder balls or solder lands, were modeled using commercially available software [23]. Construction of BGA/LGA includes package size of 35mmx35mmx2.43mm with silicon die of 13mmx13mmx0.5mm mounted on an interposer board and encapsulated with molding compound. The package is assembled with standard reflow process on a 2.28 mm thick polyimide printed circuit board. A half symmetry model was created as shown in Fig. 10 for an LGA model. Solder height varied from 500 µm for solder ball of BGA and 150 µm for solder stand-off an LGA assembly. Each material in the model was glued with tie constraints. The model was meshed using standard plain strain, 4 node, CPE4R elements. Mesh refinement was done using partitioning technique to eliminate any singularities and achieve a stable stress response. Total of 635993 nodes and 629401 elements were used in the model.

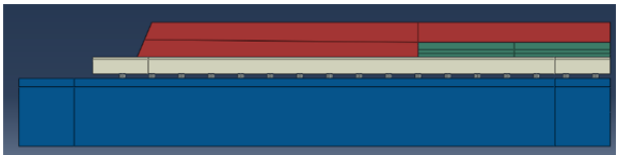

Figure 10. Finite element global modeling parameters using 2D with a half symmetry to model for LGA1156 solder assembly with stand-off 150 µm.

Figure 11 shows a typical meshed for the solder ball of a BGA assembly. In both cases of the BGA/LGA assemblies, ball symmetric boundary conditions were applied along the centerline of PCB and a pinned condition with U1=U2=0 is applied on the PCB corner to prevent free body motion. No rigid body constraints are used and the model is free to expand during thermal loads. Model is initialized at 298 K and ramped to 398 K to get the stresses due to 100 degrees temperature difference. Material properties were collected from literature for this analysis for a typical material (see Table 1).

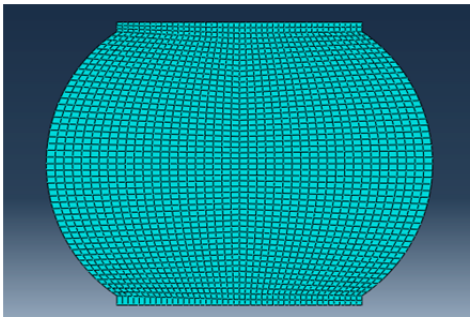

Figure 11. Meshed Solder ball for a BGA1156 assembly

Table 1. Material properties of BGA/LGA package, solder, and PCB considered for input in finite element analysis and commercial software.

Material	Temperature (K)	Elastic Modulus (MPa)	CTE (ppm/°C)	Poisson's ratio
Polyimide board	298	20684	16	0.39
Interposer	298	20684	16	0.39
Overmold	298	13000	10	0.3
Silicon	298	130194	2.5	0.3
Solder (SnPb)	238	46892	24	0.36
	258	45779	24	0.36
	278	44377	24	0.36
	295	43251	24	0.36
	398	34568	24	0.36

For tin-lead assembly, maximum stresses were observed to be 93 MPa in the outermost solder joint for the LGA and 36.68 MPa for the BGA and stresses were concentrated on the ball or solder stand-off corners. For an LGA assembly, Figure 12 shows a global stresses state, whereas Figure 13 illustrates the state of maximum stress on the outermost solder stand-off. Figure 14 shows the stress distribution in the outermost LGA solder stand-off. Several analyses were conducted at the local model level with the outermost solder stand-off for the LGA and ball for a BGA to characterize the stand-off/ball geometry, shape, and aspect ratio.

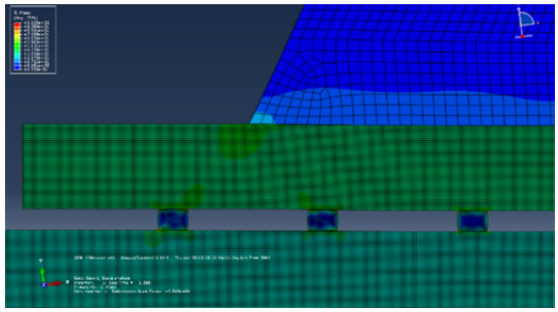

Figure 12. Global model for LGA1156 assembly showing stress concentrations on solder stand-off – outer most land with max stress

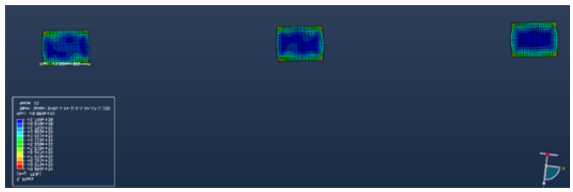

Figure 13. On the left is LGA1156 solder stand-off for the outermost land showing the maximum principal stress

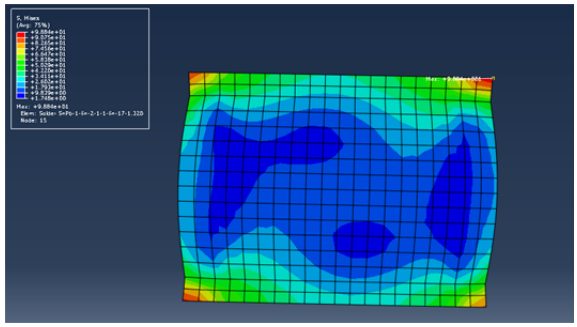

Figure 14. Outermost LGA1156 solder stand-off showing high stress location at the four corners

Commercial Software, Parametric Study for LGA/BGA 1156

The effect of various packaging aspects on cycles to failure were also carried out using a commercially available software developed based on strain energy [17, 18]. First, temperature cycling range was kept constant in the range of –55 to 100°C to determine the effects of the package ball size (LGA to BGA), die size and thickness, and other variables. Then, the effect of thermal cycling range on the BGA was considered. Both stress (MPa) and cycles to failures (50%) were presented in each plot.

Figure 15 shows cycles to 50% failure and stresses (MPa) both for the LGA and the BGA for SnPb in the graph and SAC in symbols (triangle and circle, respectively) for solder joint attachments. It is observed that solder joint height plays a critical role in solder joint reliability: the solder height was varied from 150 microns (LGA) to 500 µm (BGA). As expected, the BGA showed much higher

reliability than the LGA. Reliability is governed by shear strain that is inversely proportional to solder joint height. Larger height leads to lower strain and thus higher cycles to obtain 50% failure.

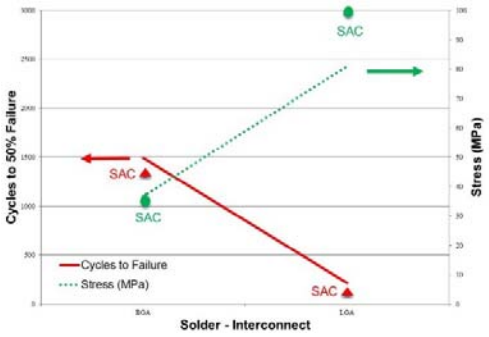

Figure 15. Effect of Solder joint height (BGA to LGA) on cycles to obtain 50% failure and stress level (MPa) for tin-lead (solid/dash lines) and SAC solder (symbols, triangle and circle)

Die size and die thickness also significantly affect cycles to 50% failure of LGA/BGA. Figure 16 shows the effect of increasing the BGA die size and Figure 17 shows the effect of increasing the BGA die thickness. Larger dies result in low cycles to failure — this is because as the die size increases, distance to neutral point (DNP) increases (see Eq. 1), and thus creates more strain in the solder joint (Eq. 2). Projection from the commercial software indicates that doubling the die size (increasing die size from 13 to 26 mm), cycles to 50% failure will decrease by about one third. Similarly, the thinner die shows better reliability as the overall package stiffness becomes more compliant and therefore induces less strain on the solder joint. Tripling the die thickness decreases cycles to 50% failure by about half.

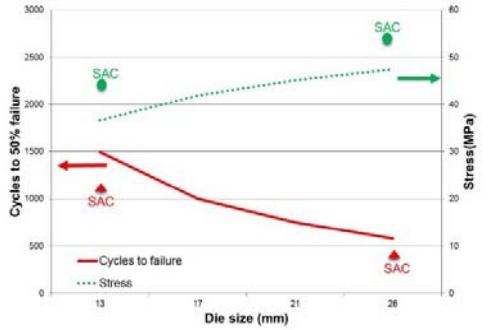

Figure 16. Effect of die size on BGA's cycles to 50% failure and stress level (MPa) for tin-lead (solid/dash lines) and SAC solder (symbols, triangle and circle)

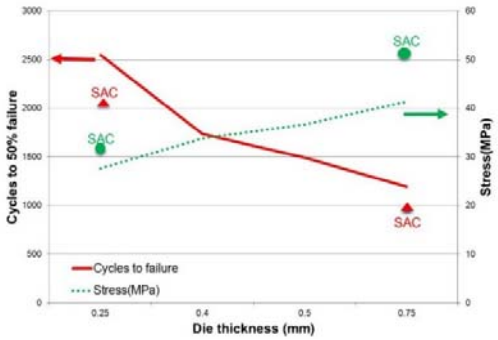

Figure 17. Effect of die size on the BGA's cycles to 50% failure and stress level (MPa) for tin-lead (solid/dash lines) and SAC solder (symbols, triangle and circle)

In addition, the effect of thermal cycling ranges were also analyzed (see Figure 18) for BGA1156. A higher delta T shows a lower reliability due to high induced strain (see Eq. 2). Increase in dwell time also resulted in reduced reliability as longer dwell solder creeping continued, but the effects beyond a level has not been settled by industry yet. SnPb solder with a liquidus of 183°C at 100°C, homologous temperature is close to 0.81 {(100+273)/(183+273)} —a figure that would cause significant creeping.

The effects of other parameters were plotted in similar graphs, but are excluded for brevity. A number of conclusions made based on exercises using commercial software are as shown in the following list.

- *CTE of PCB*: Increasing the CTE from 14 to 20 ppm showed a decrease in cycles to 50% failure from 2434 to 728, whereas stresses (MPa) increase from 29.22 to 53.44. The baseline calculation made for 16 ppm showed cycles to failure of 1494 and stress of 37.29 MPa.
- *PCB thickness*: Increasing the PCB thickness from 1.6 to 3 mm showed a reduction of cycles to 50% failure from 1575 to 1477, whereas stresses (MPa) increased from 35.36 to 38.5. The baseline for this condition is assumed to be the PCB with 2.28 mm thickness that showed cycles to failure of 1494 and stress of 37.29 MPa.
- *Effect of dwell time:* an increase from 5 minutes to 30 minutes, a decrease from 1734 to 1359 Cycles-to-failure (50%). For15 minutes, it 1494 cycles.

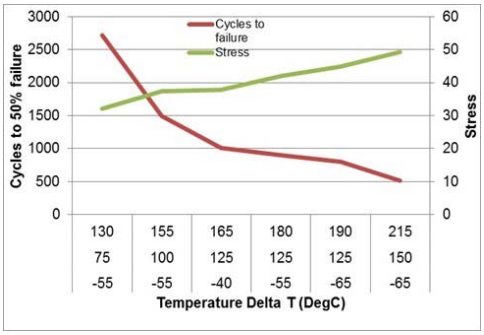

Figure 18. Effect of thermal cycling temperature ranges in order ΔT and limits (Temperature difference, High temperature limit, Low temperature limit)

MODELING CGA 1272

Unfortunately, the commercial software used has yet to include cycles-to-failure projection for CGAs, so no parametric exercise for the CGAs was performed. Data for CGAs are rare and also their use are generally limited to high-reliability applications. The significantly higher cost of the package is another contributor to lower volume. For these reason, only the FEA approach was used to determine stress distribution for the CGA1272 in order to compare the results to plastic BGA1156 version (see Figure 19 for FEA model and Table 2 for material properties).

For the CCGA 1272, the stress at the outer columns were found to be 16 MPa, which is about half of the BGA stress with balls at die edge at 36.68 MPa. The LGA had about 3 times larger stress in solder stand-off at the die edge with 93 MPa.

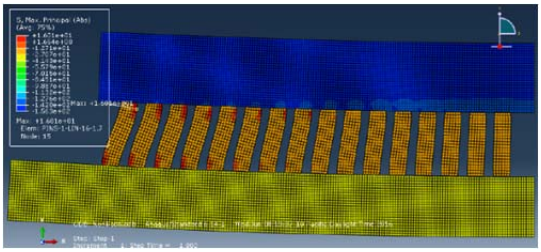

Figure 19. The CCGA 1272 Module half symmetry model (Outer columns stress 16 MPa)

Table 2. Material properties of the CGA package, column, solder, and PCB considered for input in finite element analysis and commercial software.

Material	Temperature (K)	Elastic Modulus (MPa)	CTE (ppm/°C)	Poisson's ratio
Alumina		270000	5.50	0.3
90PbSn Columns				
Polyimide board		20000	16.0	0.25
Columns	273	10879	28.50	.35
	298	9704	29.96	.35
	323	8529	29.34	.35
	348	7354	29.71	.35
	373	6179	30.09	.35
	398	5004	30.46	.35

SUMMARY

Within the last two years, the IPC/JEDEC team collaborating on guidelines on "Reliability & Design Finite Element Analysis Standard" indicate the need for more effective use of FEA. Projection approaches, as well as standardization of input parameter in FEA, are key in achieving acceptable projection of solder joint reliability with acceptable errors. Both a simple 2D FEA and the commercial software with a background theory were utilized to determine the effects of key package/board/solder parameters on assembly reliability and whether projection results reasonably agree with test results generated under various conditions. A summary of results are as follows:

- The commercial software showed projected reliability for the BGA1156 reasonably well considering most industry data are for plastic BGAs. It underestimated reliability of its LGA counterpart.
- The trends for the effect of die size and thickness are in the right direction for the PBGA as is established by industry. However, the level of changes may not agree with industry data.
- FEA was used to project the difference between BGA/LGA and CGA assembly reliability since the commercial software package covers only the BGA and possibly the LGA style packages.
- Another simple to use analytical method showed the effect of height increase for BGA vs CGA as well the effect of double-sided mirror assembly configurations for BGAs/CGAs. The current analysis projected a lower reduction in thermal cycle fatigue life for double-sided mirror-image CGA assemblies than that for BGAs. No industry data is yet available for CGA double-sided mirror image.

The FEA modeling and software analyses are considered to be a preliminary exercise. Further work on these areas should shed some light on answering questions, both by FEA and by testing, as the level of reduction in fatigue life for LGAs and methods for their reliability improvement using tin-lead solder assembly. For SAC assemblies,

literature data on the LGA indicate higher than expected assembly reliability under thermal cycling, which postulated to be due to larger grain sizes.

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