# DFX ON HIGH DENSITY ASSEMBLIES

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**ABSTRACT**
Implementing high-density assembly in all electronic products requires many considerations. Before starting any development work or implementing a new technology, it is critical to understand the product and industry requirements and capabilities. If this is not fully understood, failure is the most probable outcome.

This paper will discuss selection of the correct solder paste based on the end product and the need to conduct proper root cause analyses before making any material or process changes.

Key words: high-density assembly, solder paste selection, root cause analyses, PCB design, assembly process

**INTRODUCTION**
There are many ways to increase packaging density. Examples of technologies include fine-pitch connectors, package-on-package (PoP), fine pitch CSPs, 01005, 0201, and reduced component-to-component spacing.

Use of new technologies poses a number of challenges for solder paste selection, PCB design, assembly process, and reliability. The type of end product will have different challenges, concerns, and requirements in all aspects. The assembly line for many of these end products will look very similar, but specification limits would be different. Typical reliability tests are drop test, vibration, thermal cycling test (TCT), and SIR; even if the names of the tests are the same, the pass/fail criteria vary between different end products.

When it comes to material selection - and solder paste in particular - the type of end product plays a big role. An automotive, computing server, or router product would, in many cases, require an in-circuit test (ICT); thereby, the solder paste residues have to be easy to penetrate with a test probe. A consumer product, on the other hand, typically doesn't focus on ICT. The concern is more on throughput, thereby requiring a solder paste that is capable of fast screen printing. There are many more examples, but with the increased need for high-density assembly, most, if not all, solder pastes have to be able to print well on stencil apertures with area ratios (AR) way below the typical industry standard of 0.66. The AR for some products could be as low as 0.5-.55.

With the above challenges, finer solder powder is increasingly being used, and the type of solder powder is moving from type 3 towards type 4-4.5, and even type 5 for a number of applications. This in itself poses some new challenges. In addition, low-silver and low-temperature alloys are gaining traction, making the selection of solder pastes and alloys more complex.

Once the correct solder paste material is selected, a feasible and robust assembly process must be developed and sustained. The assembly process ranges from screen-printing, placement, and reflow soldering in air or nitrogen to electrical and functional testing. Many factors influence the quality of the assembly process. With the reduced pitch and component spacing, the capabilities for solder paste, assembly, and PCB fabrication will be tested to its limits and beyond, with the need for using statistical tools is becoming a requirement to develop and maintain good yields.

Even with the right solder paste selection, good assembly process, and high-quality PCB and components, failures still will occur, leading to yield losses and extra cost. Once these failures occur, it is very easy to jump to conclusions and start making changes without actually knowing the root cause of the failure. As engineers, we quite often tend look for the most difficult solution, but in many cases, the simple solution is the right solution to solve the issue.

## PCB AND PCBA DESIGN

When moving to high-density assembly, it is very important to understand PCB design and its limitations. With increasing density, the PCB fabrication becomes much more challenging. Some of the key PCB design requirements include:

- 50µm copper/copper spacing (inner and outer layers)
- 50µm solder mask slivers
- 25-40µm solder mask registration tolerance
- 60µm microvia's
- 200µm microvia capture pads in outer and inner layers

Understanding DFx and design is in many cases critical to be able to identify the root cause of the issues that occur on the production line. When it comes to PCB and PCBA design, there are many important aspects. In this paper, we have selected a few that have a critical impact on SPI and overall yields.

- PCB stretch and shrink
- Filled vs. unfilled microvia's
- Silkscreen

### PCB Stretch and Shrink

The maximum PCB stretch is 0.05mm over the entire panel. and this has to be clearly specified on the PCB fabrication drawing. This is very important for fine-pitch parts and high-density spacing products. The pads and apertures for 01005 passives and 0.30 mm pitch CSPs is 0.20mm; a stretch or shrink of more than 0.05mm leads to solder paste that will be 25% of the pad.

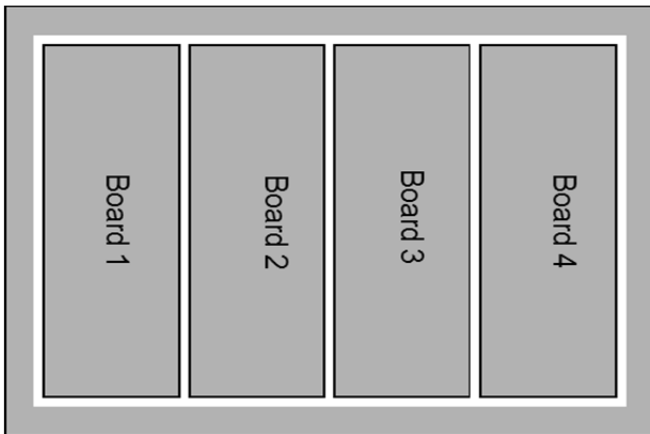


**Figure 1.** Typical PCBA panel layout for consumer products. It is important to ensure that the overall stretch/shrink tolerance is no more than 0.05mm.

### Microvia Issue

Excessive voids in some cases lead to solder bridging. This could be caused by oversized or "leaking" microvia's in pad in combination with normal process variations.

An issue on a smartphone can be seen below; failure rate for bridging was 6% in this case (Figure 2).

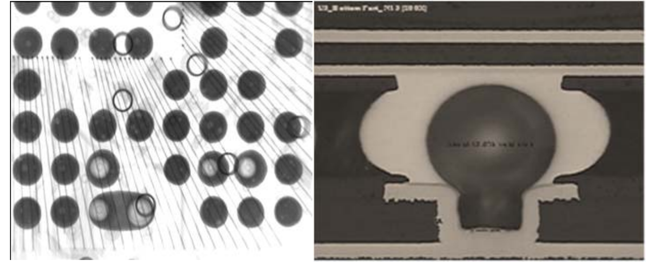

**Figure 2.** Solder bridge and excessive voids on a 0.4mm pitch CSP due to microvia size issues.

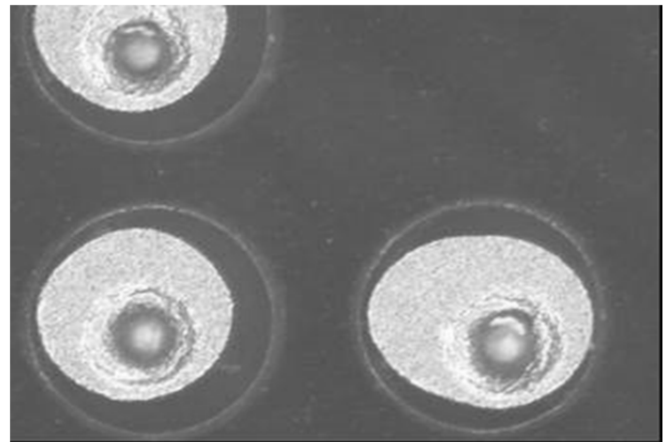

**Figure 3.** Typical unfilled microvia from top.

One primary issue today is that there are no clear specifications as to how big the microvia's are allowed to be or where to measure the actual size of the microvia (Figure 4). Since there is no clear specification, the microvia's can look different in size and shape between different suppliers and between batches of PCBs.

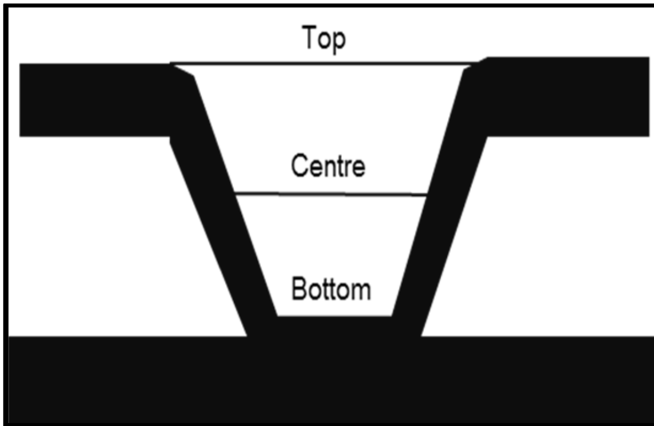


**Figure 4.** No clear specification if the microvia should be measured top, center, or bottom.

By filling the microvia's with copper in the PCB fabrication process, the voids and bridging issues can be eliminated (Figure 5).

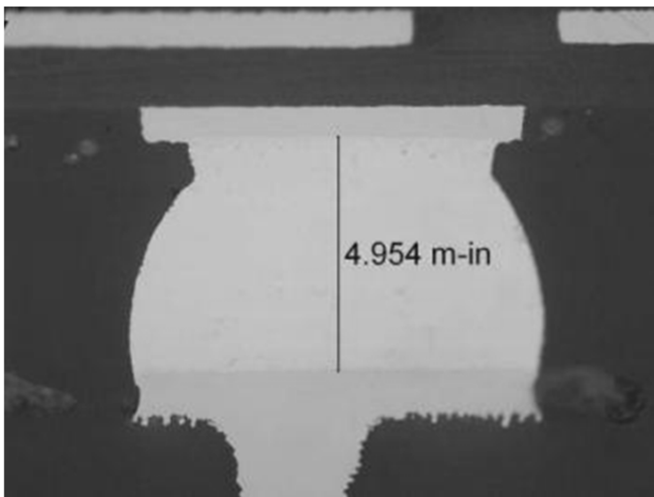


**Figure 5.** Bridge and void issue solved on a 0.40mm pitch CSP by using a copper-filled microvia.

**Silkscreen Issue**

Depending on the quality of the silkscreen, the height on top of the solder mask could range from 15-40µm (Figure 6). This can create a gap between the stencil and PCB of 15-40µm, depending on the PCB design. The gap can create printing issues leading to both too little or too much solder paste height and volume. Depending on the design of a product, the solder mask can add 10-25µm in addition to the silkscreen, creating a gap of 15-65µm from the bottom of the stencil to the pad.

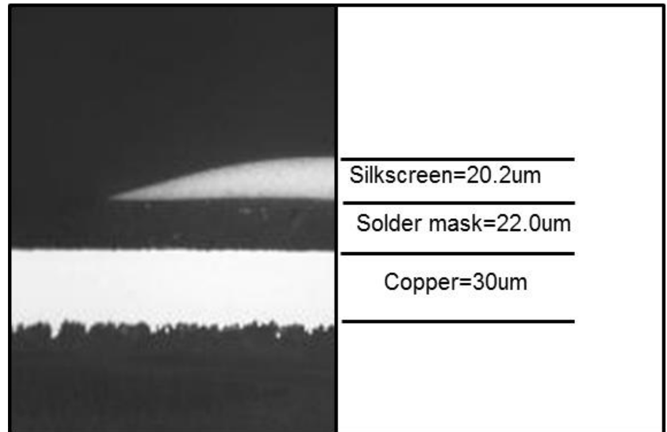


**Figure 6.** PCB silkscreen on top of solder mask and copper. In this case, the top of the solder mask is 422µm on top of the copper pad.

When the stencil is placed on top of the PCB, the effect of the silkscreen becomes very visible graphically (Figure 7). By looking at the SPI data (Figures 8 and 9), it becomes very clear that it can have a big impact on SPI yields, and potentially overall yields.

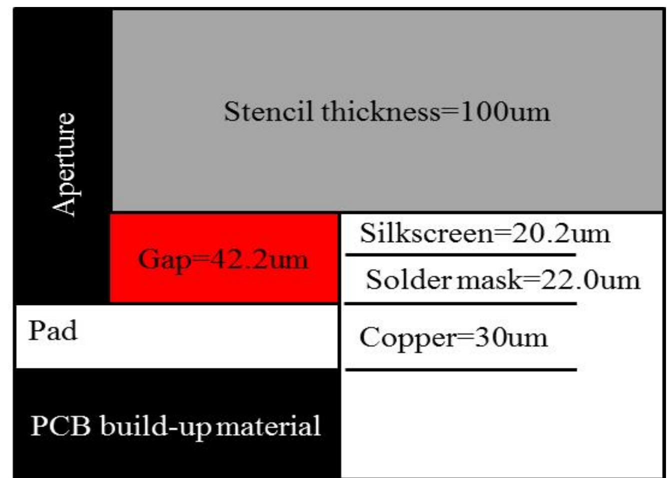


**Figure 7.** PCB silkscreen stack-up with stencil.

Silkscreen is normally not needed on today's products and is an extra cost of approximately ≈ 0,01USD/square-inch. There is also a risk that parts of the silkscreen are placed onto the pads. Copper markings should be used in the outer layers if the design can accommodate this. This applies to CSPs and other parts that have a critical placement tolerance. The effect of silkscreen on SPI performance can clearly be seen in Figure 8 and Figure 9.

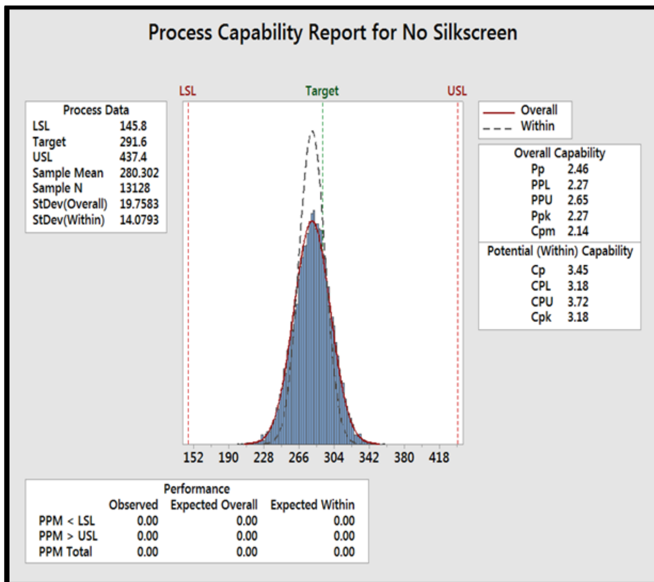

**Figure 8.** Process capability graph on a 0.4mm pitch CSP *without* silkscreen on the PCB. Volume (mil³) specification limit is 50-150%. The mean value is very well-aligned to the target volume.

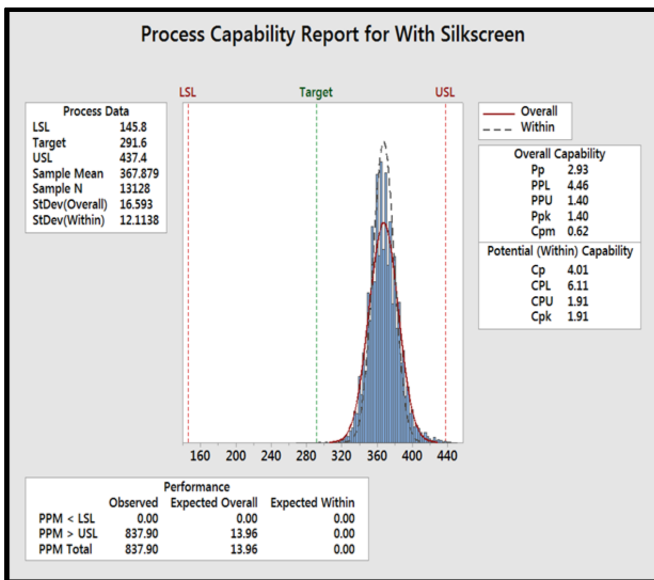

**Figure 9.** Process capability graph on a 0.4mm pitch CSP *with* silkscreen on the PCB. Volume (mil³) specification limit of 50-150%. The mean value shifted to the upper specification limit due to the impact of silkscreen.

## SOLDER PASTE AND ALLOY SELECTION

Today, the most common solder paste alloy is SAC 305 (Sn96.5/Ag3/Cu0.5) for high-density assembly technologies. When increased thermal cycling performance is required, a higher silver-content alloy such as SAC 387(Sn95.5/Ag3.8/Cu0.7) is typically used. However, using a higher silver (Ag) content alloy will increase price and could have a negative impact on mechanical reliability.

Before making the solder paste selection it is important to evaluate key material properties such as:

- Printability
- Voiding
- Cold and hot slump
- Solder balling and solder beading
- Wetting
- HIP resistance/oxidization barrier
- SIR (surface insulation resistance)

The selection of powder size varies between type 3, type 4, type 4.5, and type 5 (Table 1). With the correct flux formulation, a more expensive type 5 powder can in many cases be avoided but still meet an acceptable Cpk of 1.67 (Table 2). Besides a cost increase, type 5 powder also increases the risk of HIP and graping due to an increased surface area and oxide content. Even though reflow in air is possible, nitrogen reflow is most common in the market for type 5 powders.

**Table 1.** Powder types according to J-STD-005

| Powder Type J-STD-005 | Size Range (micron) | |
|---|---|---|
| 3 | 25 | 45 |
| 4 | 20 | 38 |
| 4.5 | 20 | 32 |
| 5 | 15 | 25 |

**Table 2.** Cp and Cpk comparing type 4.5 and type 5 powder on a 0.2x0.2mm aperture and 0.08mm thick stencil (AR=0.625).

| FLUX | Powder | Cp | Cpk |
|---|---|---|---|
| A | Type 5 | 2.2 | 2.18 |
| A | Type 4.5 | 1.82 | 1.81 |
| B | Type 5 | 2.05 | 2.04 |

## PROCESS

From a process point of view, screen printing has always been seen as the major contributor of yield loss. Many investigations over the last few years have shown that printing can contribute to 60-70% of the overall process yield loss, followed by reflow soldering ranging between 10-20%.

### Voiding, Graping, and HIP

Recently, QFN voiding has become a very hot topic. In some cases, reducing QFN voiding can be done with the help of a hot and long soak, burning off more flux residues that could lead to excessive voiding.

The drive for reduced QFN voiding can lead to an increase of graping on 0201 and 01005 passive parts and also an increase of head-in-pillow (HIP) on fine-pitch CSP's and

PoP's. Many studies show that graping does not have a negative impact on shear strength, but it is a clear process indicator for HIP. In both cases, flux exhaustion is caused by excessive heat and time before the solder joints are formed.

With regards to HIP, there are also other factors such as warpage and ball/bump contamination that impact the total amount of failures.

The head-in-pillow defect (Figure 10) is an open solder joint in a BGA or CSP where the solder paste deposit does not coalesce to the ball on the component. The result is an apparent solder joint with a gap between the solder reflowed to the PCB paste and the solder ball itself. This defect is particularly troublesome because it is very difficult to detect, even with X-ray inspection.

In addition, sometimes there is mechanical contact between the two solder deposits allows it to pass functional testing but it fails later in the assembly process or in worst case on the field.

**Figure 10.** Typical HIP issue when using too long soak time and too high soak temperature. This issue could pass a functional test and end up as a field return.

Graping (Figure 11-12) is also in many cases referred to as cold solder. Not understanding the true root cause of the issue drives a different set of potential process solutions that in many cases magnifies the issue.

**Figure 11.** Graping illustration

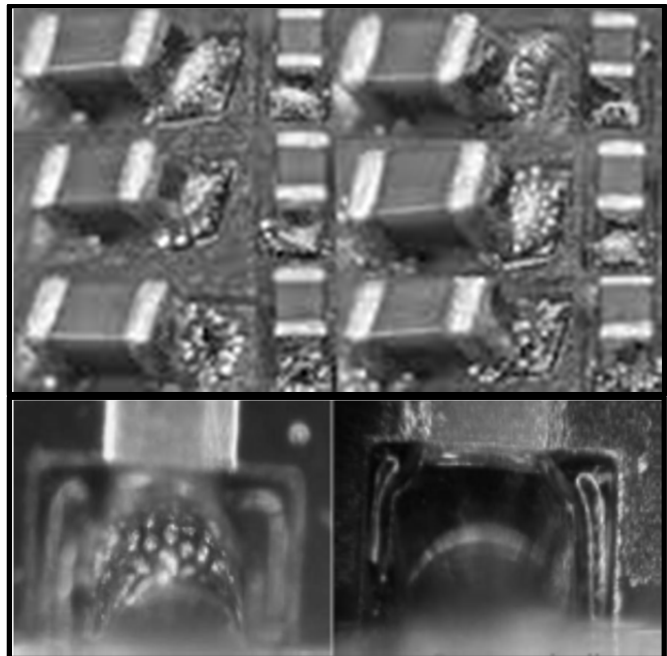

**Figure 12.** Actual images of graping of 01005 components (top and lower left), and a good solder joint on 01005 lower right).

Graping typically happens on smaller solder paste deposits (Figure 13) due to fact that the smaller amount of solder pastes results in smaller amounts of flux to remove oxides.

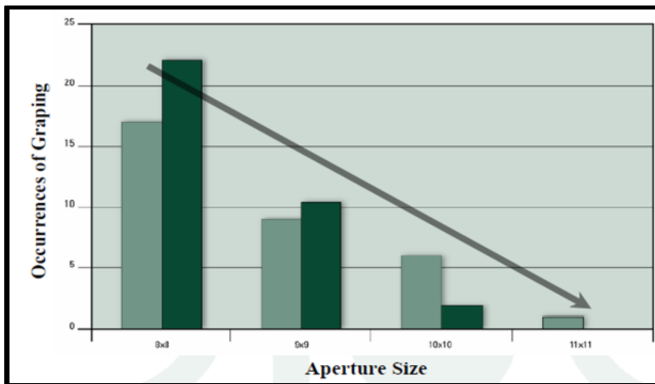

**Figure 13.** Impact of aperture size on amount of graping.

In IPC 610 section 1.5.2, the following definition can be found:
*"Cold Solder Connection - A solder connection that exhibits poor wetting and that is characterized by a grayish porous appearance. (This is due to excessive impurities in the solder, inadequate cleaning prior to soldering, and/or the insufficient application of heat during the soldering process.)."*

In section 5.2.5, this is further explained by including rosin connection. Cold and rosin connections are both classified as a defect for IPC class 1-3.

In section 5.2.3 of IPC 610 Soldering Anomalies – Reflow of Solder Paste, incomplete wetting is classified as a defect for IPC class 1-3.

Below is an example using a 0.40mm pitch CSP with 0.25mm round apertures and a 0.10mm thick laser-cut stencil. This shows that, by increasing the ramp rate above 180°C from 0.7°C/s to 1.2°C/s, the HIP defect detected in functional testing is reduced from 1.5% to 0% (Table 3).

**Table 3.** Yield loss on an actual product at different ramp rates and in air vs. nitrogen reflow for a 0.4mm pitch CSP.

| Ramp rate 180-220˚C (˚C/s) | Yield Loss (%) |
|---|---|
| 0.7 (air reflow) | 1.5 |
| 0.7 (Nitrogen reflow) | 0 |
| 1.2 (air reflow) | 0 |

In this case, nitrogen (<1000ppm of $O_2$) reflow (Table 3) has the same positive effect on the functional yields. One thing to keep in mind is that this is functional test yield loss, and many HIP defects might not be captured because there could be marginal mechanical and electrical connections.

Another common mistake is using 217°C as the liquidus temperature for SAC 305 and SAC 387. The liquidus temperature for SAC 305 and SAC 387 is actually 220°C and it is the solidus that is 217°C.

This can lead to some confusion when setting the specification limits for the reflow profile. If the plateau is between 219-220°C, this can lead to severe flux exhaustion resulting in graping and HIP in hip-scale packages (CSP) and package-on-package (PoP).

**Table 4.** Liquidus and solidus temperatures for SAC 305 and SAC 387.

| Alloy | Temperature ˚C | |
|---|---|---|
| | Liquidus | Solidus |
| SAC 305 | 220 | 217 |
| SAC 387 | 220 | 217 |

**Inspection Tools for Voiding, Graping, and HIP**
There is no set requirement for the QFN voiding limit, and each company has their own specification. The range can vary between 15-50% for standard applications and down to 5% for special applications.

X-ray is the most common way to verify the voiding levels, and most modern X-ray equipment will do an accurate void calculation.

The issue is that many production lines worldwide do not have adequate high-magnification microscopes to validate that the void reduction don't have a negative impact on solder joint quality.

IPC 610 clearly specifies that the minimum magnification required for solder joints <0.25mm should be 20X, and in many cases, only a 2-4X magnification glass is available; a graping issue would easily be missed when using 2-4X magnification glass.

**CONCLUSION**
It is very important to understand design, materials, and process since they are very closely connected. There are many ways to achieve high-density assemblies, and it is crucial to have a "toolbox of technologies" to be able to fulfil various requirements. It is also necessary to consider the interaction between multiple technologies in all areas during development and deployment since several advanced technologies will, in most cases, be used on the same product. Depending on the end product, several options can be considered and the selection should be based on data and not assumptions.

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