

BOARD LEVEL RELIABILITY OF FINE PITCH FLIP CHIP BGA PACKAGES FOR AUTOMOTIVE APPLICATIONS

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ABSTRACT

The drive for higher performance and smaller electronic components make flip chip ball grid array (FCBGA) packages attractive for automotive applications. As automobiles rely more heavily on electronics for passenger safety, efficiency, and comfort, component reliability has become increasingly important. Since automotive components operate in extreme environmental conditions, with a temperature range of -40°C to $+125^{\circ}\text{C}$, solder joint reliability of ball grid array packages is a major concern in automotive systems. Because of the difference in thermal expansion of the different packaging materials and the printed circuit board (PCB), temperature variations create thermal mismatch, resulting in solder joint stress. After repeated thermal cycling, the solder joints can crack and lead to system failures.

In our study, the board level reliability of different FCBGA packages was evaluated in the automotive thermal cycling environment. The effect of different factors, such as package construction, underfill type, and ball pitch, have on board level reliability of flip chip packages will be discussed. Our studies showed FCBGA packages using organic substrates can achieve high board level reliability under automotive operating conditions.

Key words: flip chip, ball grid array, automotive, board level reliability; solder joint fatigue

INTRODUCTION

Flip chip technology offers the advantages of high pin count, enhanced electrical performance, and excellent thermal characteristics. Typical flip chip packages are either bare die or lidded, as shown in Figures 1 and 2. The bare die package has the advantage of lower cost and smaller package stress while the lidded package offers better die protection and package warpage. Although flip chip ball grid array packages have been widely used for consumer and mobile applications, they are still relatively new for automotive applications. As the automotive industry is looking for high performance, low cost packaging solutions, flip chip is becoming more attractive. However, its use may be limited due to solder joint reliability concerns in harsh environments with extreme temperatures excursions.

With the need for lead-free materials to meet environmental requirements, the board level reliability challenges are more difficult. Since lead-free alloys require higher reflow

temperatures for assembly than the conventional tin-lead eutectic alloy, the use of lead-free solders places higher demands on package materials [1-2]. Lead-free solder bumps are brittle and have less solder fatigue resistance during thermal stress, so a higher glass transition temperature (T_g) underfill is required for bump crack protection in flip chip devices [3]. The higher T_g underfill can increase package warpage and induced more stress on the BGA solder joints, which can affect the overall package reliability.

When a temperature change occurs, the thermal expansion difference between the component and printed circuit board (PCB) results in stresses and strains on the solder ball joints. Eventually, continuing thermal excursions will result in solder ball fatigue failures. As the temperature range for the thermal cycling increases, the solder joint strain increases, which leads to a decrease in the thermal fatigue performance of the package. Significant reductions in solder joint fatigue life have been reported in temperature cycling tests, especially under harsh accelerated conditions such as -40°C to 125°C [4-6].

This paper presents the results of board level reliability assessments for different flip chip BGA packages. The impact of a lid and different underfills on package warpage and solder ball fatigue life using an accelerated thermal testing condition of -40°C to 125°C was evaluated.

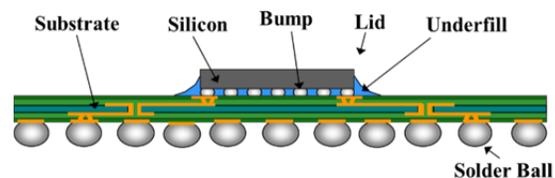


Figure 1. Cross section of a flip chip bare die BGA package

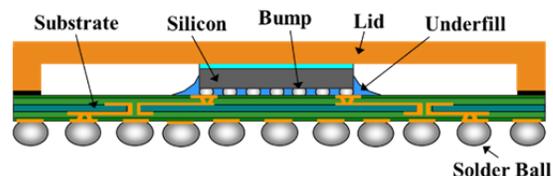


Figure 2. Cross section of a flip chip lidded BGA package

EXPERIMENTAL

Package Description

Five different flip chip test vehicles were used in the study, including 19 mm and 23 mm package body sizes. The devices were assembled with 9.1 X 9.7 mm² ultra low-k die on build-up laminate substrates. The 23 mm packages had 1.0 mm BGA pitch with 0.6 mm solder balls while the 19 mm packages had 0.8 mm pitch with 0.5 mm diameter solder balls. The test vehicles had either a bare die or lidded construction. The key attributes of the test vehicles are summarized in Table 1. All packages used for board level testing had a daisy chained connection between the substrate solder ball and the board so that the solder ball resistance between the package and the board could be monitored. All the test vehicles were assembled using eutectic bumps and SnAg3Cu0.5 (SAC305) BGA solder balls. The substrates had solder mask defined (SMD) pads and a Cu SOP pad finish. The lidded package used a single piece copper lid attached to the substrate with an epoxy material and thermal interface material (TIM) between the die and the lid for improved thermal performance.

Two different underfill materials that varied in Tg were evaluated during this study. Underfill A (UF-A) had a low Tg, which is good for low-K dielectric protection and package warpage control while underfill B (UF-B) had a high Tg and is better for lead-free bump protection. The underfill properties are shown in Table 2. Prior to the board level study, extensive package level testing was performed to ensure the robustness of the packaging materials and design to withstand extreme environmental conditions. All the package types passed JEDEC standard package reliability tests (preconditioning with MSL-4, 1000 hours of Temperature Humidity Bias (THB), 1000 hours of High Temperature Storage (HTS), and 1000 cycles of thermal cycling (-55°C-125°C)) without any die or package related issues. Lead-free bumped devices assembled with underfill B was able to pass 1000 cycles of temperature cycle testing without any bump cracking or die delamination.

Table 1. Test Vehicle Attributes

Test Vehicle	TV1	TV2	TV3	TV4	TV5
Package Type	Bare Die	Bare Die	Lidded	Bare Die	Bare Die
Package Size (mm)	23X23	23X23	23X23	19X19	19X19
Die Size (mm)	9.1X9.7	9.1X9.7	9.1X9.7	9.1X9.7	9.1X9.7
Ball Count	484	484	484	484	484
Underfill	UF-A	UF-B	UF-A	UF-A	UF-B
Ball Pitch (mm)	1.0	1.0	1.0	0.8	0.8
Ball Size (mm)	0.6	0.6	0.6	0.5	0.5
Ball Alloy	SAC305	SAC305	SAC305	SAC305	SAC305
Substrate Thick (mm)	0.95	0.95	0.95	0.95	0.95

Table 2. Underfill Properties

Item	Unit	UF-A	UF-B
Tg, (TMA)	°C	70	100
CTE, <Tg	ppm/°C	36	26
CTE, >Tg	ppm/°C	120	100
Modulus, <Tg	GPa	8.5	10
Modulus, >Tg	GPa	0.04	0.10

Test Boards

The packages were assembled onto 290 mm x 140 mm test boards with a thickness of 2.4 mm. The test boards had 8 layers with simulated ground and power layers with a 70% metal distribution and signal layers with a 40% metal distribution. The boards were made of high Tg FR4 material and had non-solder mask define (NSMD) solder pads with organic solderability preservative (OSP) surface finish. Each board had eight package sites for assembly. Test points were incorporated in the daisy chain design to help isolate the failure locations.

Warpage Characterization

Prior to board level assembly, the packages were measured for coplanarity at room temperature using a RVSI system and warpage variation over temperature was collected using shadow moiré for the different packages. The samples were measured from room temperature up to 260°C and then back down to room temperature.

Thermal Cycling Tests

The test boards with the mounted packages were subjected to thermal cycles over the range -40°C to 125°C, and the daisy chain resistance of the components was monitored throughout the testing with an event detector. Each cycle consisted of 10 minutes dwells at the low and high temperatures and 10 minutes ramps. When the daisy chain in-situ resistance exceeded 500 ohms during thermal cycling, it was logged as an open failure. Detailed failure analysis was performed to locate the failure modes and locations.

TEST RESULTS AND DISCUSSION

Package Warpage Comparison

The coplanarity values of the different packages are shown in Figure 3, with the 19 mm packages having better coplanarity than the larger 23 mm packages. Devices assembled with the low Tg underfill (UF-A) showed lower coplanarity than the ones with the high Tg underfill (UF-B). Devices with a lid were more rigid and had better coplanarity compared to the bare die packages. For the 23 mm package, a lid reduced the average coplanarity 35% from 2.0 to 1.3 mils for TV1 and TV3, respectively.

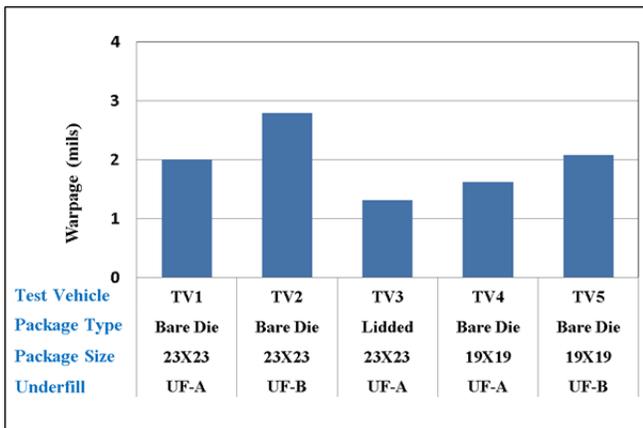


Figure 3. Package Coplanarity

Shadow moire testing was also performed to evaluate the warpage variation over temperature. The samples were measured from room temperature up to 260°C and then down to room temperature as shown in Figure 4. According to JEDEC STANDARD JESD22B112, “High Temperature Package Warpage Measurement Methodology,” a negative measurement value indicates that the package is concave meaning the package corners are higher than the center with respect to the seating plane while a positive value indicates the package is convex with the package corners lower than the package center [7]. From the shadow moire data, the bare die package had a convex (crying) curvature throughout the heating and cooling cycle, with the high Tg underfill units having higher warpage compared to the low Tg underfill devices. The addition of the lid not only changed the warpage curvature to concave (smiling) but also reduced warpage variation during thermal cycling loading.

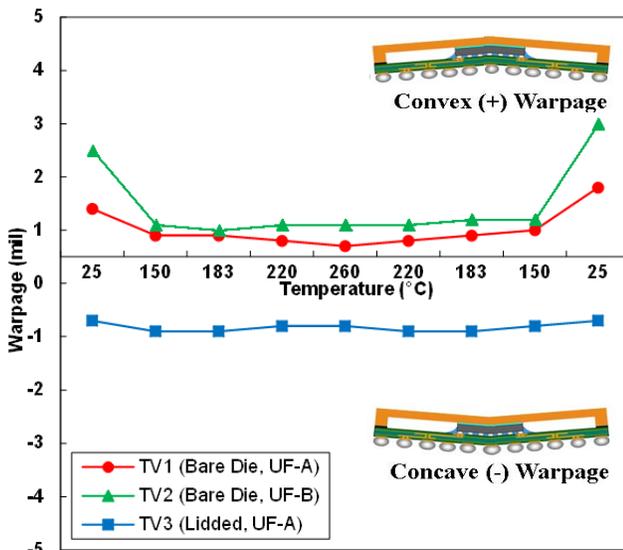


Figure 4. Warpage change with temperature for the 23 mm packages.

Thermal Cycling Test Results

The assembled test boards were subjected to -40°C to 125°C thermal cycling. A sample size of 32 units for each package type was used. The failure cycles for each package were recorded and the accumulated failures were analyzed using a two-parameter Weibull distribution. The temperature cycle data is summarized in Table 3. The characteristic life (Eta) is the number of cycles at which 63.2% of the sample set has failed. The failure rate of the test vehicles is described by the slope, Beta. In general, higher Beta values indicate faster failure rates or shorter time between failures.

Table 3. ATC results for the test vehicles.

Test Vehicle	Package Type	Package Size (mm)	Underfill	1st Failure (cycle)	Char Life (cycle)	Beta
TV1	Bare Die	23X23	UF-A	2982	3864	11.3
TV2	Bare Die	23X23	UF-B	1761	2261	13.2
TV3	Lidded	23X23	UF-A	3009	5307	7.7
TV4	Bare Die	19X19	UF-A	3912	4890	14.3
TV5	Bare Die	19X19	UF-B	2322	2682	18.0

23 mm Package Temperature Cycle Results

The temperature cycling results for the 23 mm packages with 1.0 mm BGA pitch are shown in Figure 5. As shown, the package construction and the underfill type had significant effects on the board level reliability. The 23 mm bare die package with the low Tg underfill had the first failure at 2982 cycles and a characteristic life of 3864 cycles. However, using a high Tg underfill decreased the characteristic life about 42% to 2261 cycles. Since the packages were constrained on the PCB, the devices with the higher warpage behavior resulted in larger tensile stresses to the solder balls near the center of the package and caused earlier failures. The application of a lid not only improved package warpage but also increased board level life. Packages assembled with low Tg underfill and a lid (TV3) had a 27% improvement in solder joint life compare to the bare die devices.

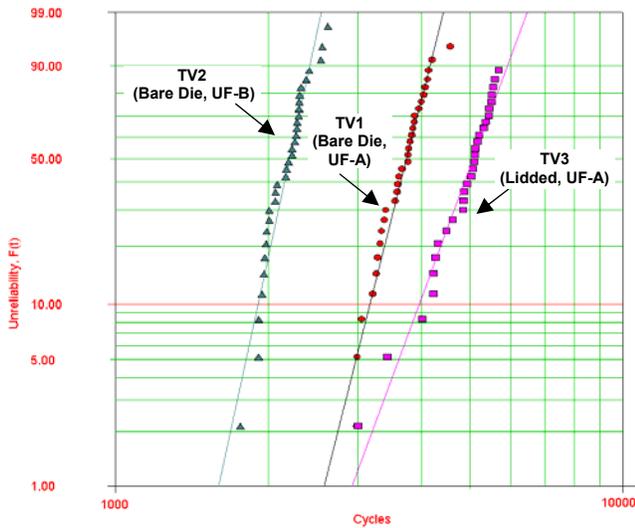


Figure 5. Weibull Plots of the 23 mm packages

A detailed analysis on the extent and location of the solder joint failures on each package was performed using dye and pry on each leg. Figure 6 shows the dye and pry maps for the 23mm packages at 2000 cycles and 3000 cycles, where the solder joint locations that are almost fully cracked are indicated by red. At 2000 cycles, the high Tg underfill leg (TV2) started failing while the low Tg underfill legs (TV1 and TV3) were still passing. However, at 3000 cycles, only the lidded package (TV3) was able to pass. The dye and pry results showed solder ball cracks occur mainly under the die area of the package, where the solder balls have the highest stresses. The cross section of the solder joints showed solder ball cracking at the solder-package interface as shown in Figure 7.

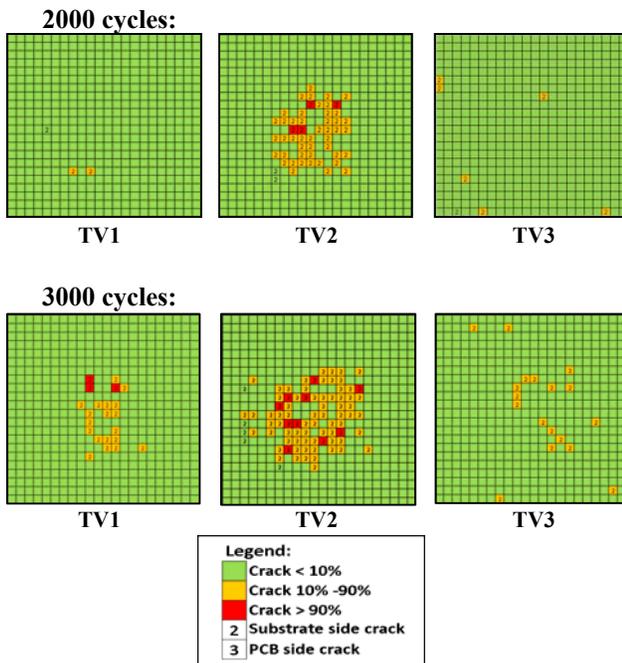


Figure 6. 23 mm Package Dye and Pry Solder Joint Failure Plots

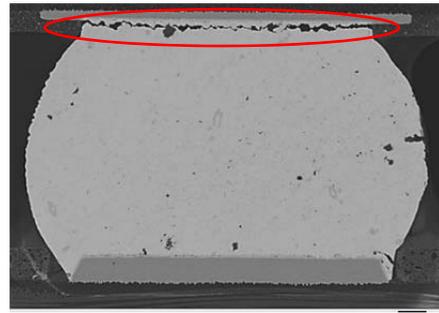


Figure 7. Cross section of BGA of 23 mm package.

19 mm Package Temperature Cycle Results

The temperature cycle results of the 19 mm packages are shown in Figure 8. The TV4 devices with the low Tg underfill had the first failure at 3912 cycles while the TV5 devices with high Tg underfill had the first failure at 2322 cycles. For the 19mm devices, using the high Tg underfill decreased the board level characteristic life by 45%. Dye and pry analysis on the first failure units showed that solder joint cracking were located mainly under the die area of the package as shown in Figure 9. The die tends to influence the localized CTE of the package substrate causing higher stresses on the solder joints under the die area. The cross section of the solder joints near the die edge showed solder joint cracking near the package interface as shown in Figure 10.

A comparison of the characteristic life showed that the 19 mm package had better board level performance than the 23 mm package. Although both the 19 mm and 23 mm packages had the same die size and solder ball count, the 19 mm package had a smaller solder ball pitch and diameter ball. Smaller solder joint diameter and height typically decrease fatigue life since they decrease the load bearing area and increase the shear strain in the solder joint. However, the 19 mm package with the smaller ball pitch had an increased number of solder balls under the die to share the load. Increasing the solder ball density under the die decreased the stress per ball and improved the board level reliability.

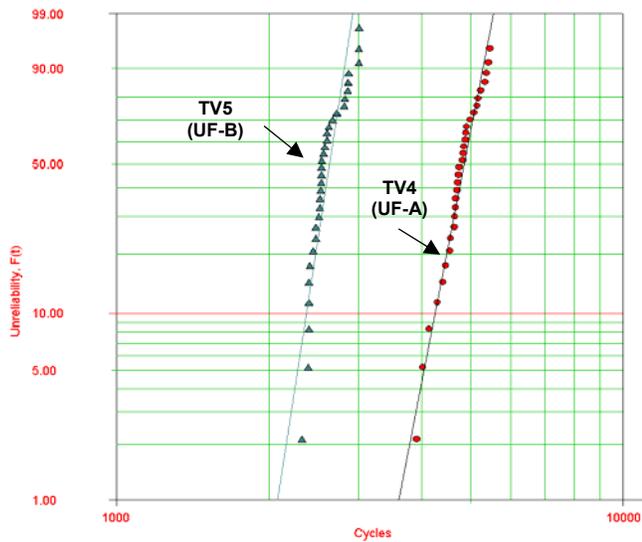


Figure 8. Weibull Plots of the 19 mm packages.

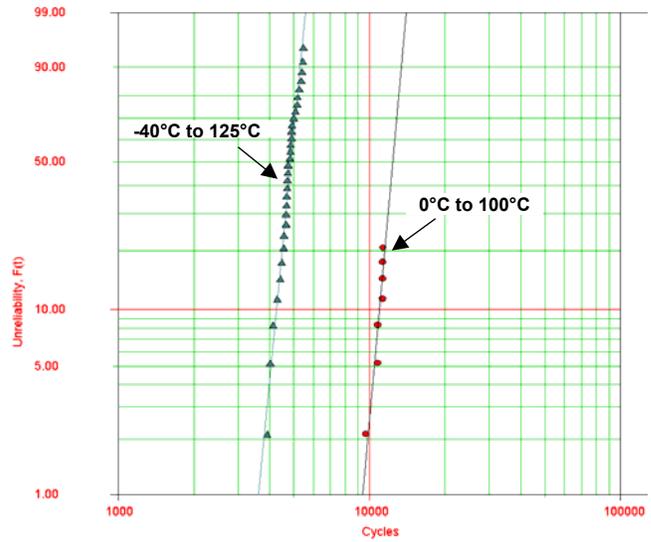


Figure 11. Weibull Plots of the TV4 at different ATC conditions.

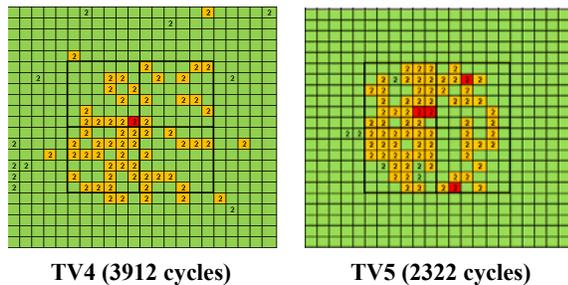


Figure 9. 19 mm Package Dye and Pry Solder Joint Failure Plots of the first failure of each package.

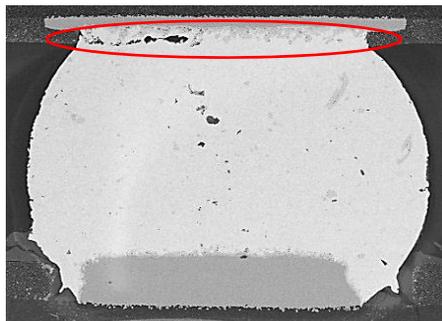


Figure 10. Cross section of BGA of 19 mm package

The TV4 devices were also tested to the common milder thermal cycling condition of 0°C to 100°C to understand the acceleration factor for different temperature cycle conditions. The board level test results are shown in Figure 11. From the data, the units tested at the -40°C to 125°C condition had a characteristic life 2.6 times worse than units tested at the 0°C to 100°C condition. The higher temperature extreme resulted in greater strain to the solder joints and negatively affected the solder fatigue life.

CONCLUSION

In our study, the board level reliability of flip-chip BGA assemblies on laminate substrates was evaluated for automotive use by temperature cycling -40°C to 125°C. The influence of assembly materials and package design on package warpage and board reliability was presented. The results showed that samples assembled with higher Tg underfill had a negative effect on warpage and thermal fatigue solder ball life of the flip chip packages. Lidded packages reduced warpage variation during thermal cycling loading and resulted in higher board level reliability compared to the bare die package. For the same die size and package ball count, reducing package size by reducing the solder ball pitch and increasing the ball density under the die resulted in higher board reliability. This suggests that package miniaturization by moving to a finer ball pitch could be a feasible lower cost package option. An increase in the thermal cycling range decreased the number of cycles to failure for the solder joints due to fatigue. Thus, proper selection of package materials and design is necessary to achieve high board level reliability in high temperature applications.

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