BTC/QFN TEST BOARD DESIGN CONSIDERATIONS AND METHOD FOR QUALIFYING SOLDERING MATERIALS AND CLEANING PROCESSES

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ABSTRACT

It becomes necessary from time to time to change materials of construction, manufacturing processes, and process conditions. A soldering material or cleaning agent may become unavailable due to environmental regulation, market forces, or reformulation. The following conditions necessitate validation and verification:

1. New soldering and / or cleaning materials changes that may improve performance or be more cost effective.
2. New soldering or cleaning equipment.
3. Technology assembly advances using a wide range of components placed in highly dense footprints.

Each of these conditions require some form of verification and validation that the process meets the Original Equipment Manufacturers (OEMs) quality and reliability specifications.

J-STD-001 Requirements for Soldered Electrical and Electronic Assemblies states that validation and verification be confirmed with test vehicles that are representative of the product being produced. Many of the industry standard test vehicles are dated and not representative of current electrical and electronic assemblies. The purpose of this research is to use a non-standard test board with sensors placed at the bottom termination to study cleanliness and contamination effects under QFN components. The non-standard test board has features to also study thermal paddle design options and to develop a risk profile. This research will report Surface Insulation Resistance effects at the source of the residue.

Key words: Bottom Terminated Components, J-STD-001, Flux Residues, Reliability, Warranty, Surface Insulation Resistance

INTRODUCTION

High density interconnected printed circuit assemblies are increasing the use of surface mounted Bottom Terminated Components (BTCs). BTCs contain external metallized terminations under the component body. Planar pad surfaces using a range of surface finishes are common. Surface finish, standoff gap, thermal vias, solder paste flux composition, stencil selection, and thermal profile are factors that can influence the properties of soldering residues present under the component termination.

BTCs are low cost components and available in different design configurations and sizes. Circuit designers are using more BTCs due to the small footprint and minimal Printed Circuit Board (PCB) area requirements [1]. Benefits include increased product functionality using smaller form factors, low profile, finer contact pitch, and higher component placement densities.

Lower package thickness and finer pitch BTC components improve electrical and thermal performance. The tradeoff is a lower standoff height. As standoff heights reduce, flux residues can become trapped under the component termination [2]. When flux is void of outgassing channels, a number of reliability issues can arise, even when using a no-clean solder paste [3].

1. The level of flux residue under the component increases
2. Flux activators are not properly outgassed
3. Flux bridges power and ground connections
4. The risk of leakage currents are significantly increased.

The purpose of this research is to use a site specific QFN test board for determining the activity of flux residue under the component interface. The research will evaluate design options at the thermal paddle (ground lug) and thermal pads to improve flux outgassing, increase standoff and reduce the level of flux residue trapped under the bottom termination. Residue trapped under the QFN is very difficult to clean. Extended cleaning time is often necessary to remove all residues. If errant flux is not totally cleaned, there is a risk of failure when the device is used within harsh environments.

QFN DESIGN OPTIONS TO REDUCE RESIDUES

BTC packages do not have solder ball terminations. The electrical connection between the package and the assembly board is made from solder interconnection of the component to the circuit board. Package considerations include surface

finish, solder paste volume, solder mask definition, thermal vias, solder mask windows, silk screen dots, solder paste flux composition; reflow profile and cleaning. The assembly processes for attaching BTCs requires careful process development and control.

Surface Finish

Hot Air Solder Leveling (HASL), the standard finish for tin-lead boards, provided excellent solderability by wetting the underlying copper pad. An intrinsic benefit of HASL finish was the natural elevation of the component from the board surface. This 20-50µm extension, provides a channel for flux to outgas during reflow. This standoff elevation reduces flux residue, with the residue being tightly constrained next to the solder pads [2]. Low standoff gaps result in heavy flux accumulation under the component termination resulting in flux residue bridging and underfilling the bottom termination.

With the widespread use of BTCs and other fine pitch devices, increased control of PCB flatness was needed. Planar surface finishes were used to solder the BTC to the circuit assembly. Plated pads result in less variability over the hot air solder leveling process. A couple of tradeoffs in regards to contamination include: 1.) Planar pads result in lower standoff. & 2.) The oxidation layer present on the component finish varies. Some component finishes require higher flux activation to achieve needed solderability yields.

Solder Paste Thickness Printed on Thermal Pads and Paddle

For QFN components, the solder joint standoff is a direct function of the amount of solder paste thickness on the thermal pad and the type of vias used in the thermal paddle area [1]. Board mounting studies have shown that the package standoff increases by increasing solder paste thickness and by using plugged vias in the thermal paddle region. An open via provides a path for solder to flow into the PTH and decreases package standoff height while a plugged via impedes the flow of solder into vias.

Solder Mask Definition

Solder mask definition strategies are also worthy of design consideration. Non-Solder Mask Defined (NSMD) lands has an opening that is slightly larger than the land geometry. During reflow, flux has a channel to outgas. This strategy reduces the level of flux residue present post soldering [4]. Solder mask defined (SMD) places a small trace of solder mask over the land geometry. Using this strategy, flux does not have a channel to outgas. Higher levels of flux will be trapped under the component termination. No-SM (no solder mask) lands remove all the solder mask around the land geometry and under the component termination. See Figure 1. No-SM increases the distance from the board to the bottom side of the component. No-SM strategy reduces flux accumulation and facilitates an easier to clean condition.

Thermal Vias

Thermal vias placed within the thermal paddle provide a flux outgassing channel. Channels that allow flux to outgas and escape the thermal paddle area reduce flux residues in the streets (or plus-sign pattern shown in Figure 1) and pad region [3]. Voids are reduced due to the flux gas exhaustion during solder reflow. One issue is solder wicking inside thermal vias. Solder that is permitted to wick into vias has the potential of flowing to the opposite side of the board, creating an opportunity for unintended electrical connections. To address this issue, one possibility is to use non-plated vias. A second design consideration is to use solder mask windows placed within the thermal paddles.

Solder Mask Windows

This approach combines conventional through-hole vias with custom solder mask windows within the thermal pad area (Figure 1). The use of solder mask windows can help reduce part-to-part variation. The thermal vias placed in the solder mask window reduces the potential of solder wetting vias. Solder paste does not wet to solder mask. The solder mask windows within the thermal paddle remain confined to the area from which the solder paste has been printed. During reflow, the flux gases have a channel to outgas. There is a higher potential for the flux to be properly heat activated, rendering a benign residue after reflow. By properly encapsulating and drying out the flux residue, there is less potential for high resistance shorts and leakage currents.

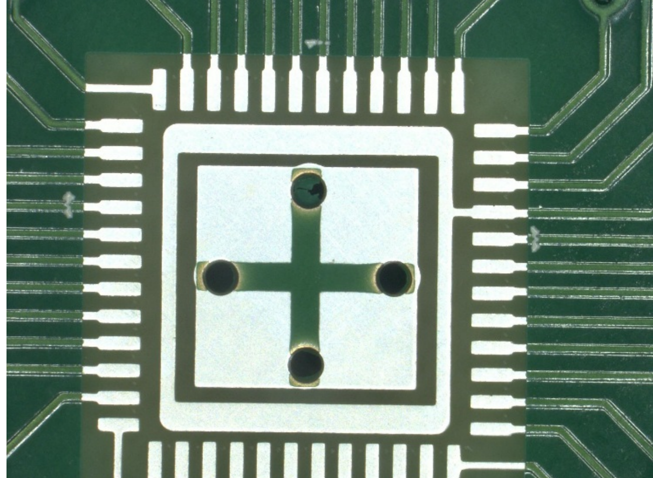


Figure 1: Solder Mask Window Example with Non-Plated Vias

Silk Screen Dots

The use of silk screen dots at the four corners of the component offers the potential to increase and maintain a minimum standoff height. The intent of this design feature is to prevent the component from fully collapsing onto the surface of the board during reflow. The silkscreen marking is designed to provide a mechanical stop and height reference during and after assembly. See Figure 2.

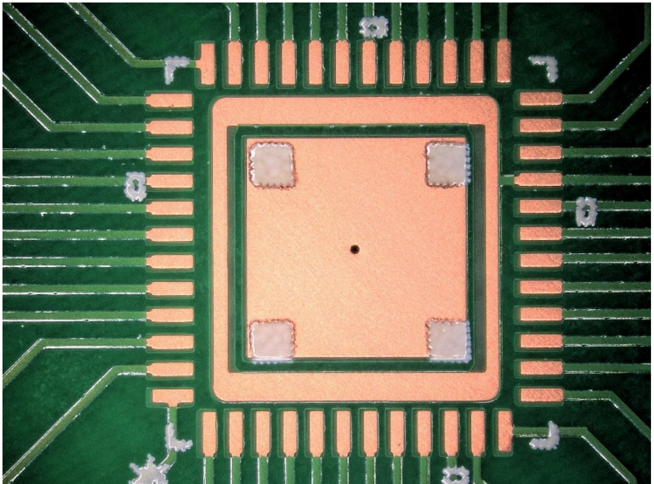


Figure 2: Silk Screen Dots Designed to Increase Standoff Gap

Solder Paste Composition

No-Clean flux residues, by design, can create resistive connections between pads on BTC packages. If a low residue, no-clean solder paste is used, the design feature of this solder paste is that PCB cleaning is not required and the remaining residue has little effect on the reliability of a BTC. No clean fluxes and solders simply mean that there are no harmful residues left on the board that could cause corrosion or damage to the components if left on the board surface.

To render the flux benign (no-clean state), requires solvents within the flux to evaporate, decomposition of certain flux ingredients, and encapsulation of metal oxides and other potentially active flux ingredients [5]. Large voids in the thermal paddle and trapped residues that are mobile after reflow soldering creates significant risk of leakage and dendritic growth, even when using a no-clean solder paste.

Each board has a different thermal mass. Dependent upon component placement and distribution of copper planes on each side of the board, the reflow profile must be dialed in to assure proper wetting, solder joint formation and flux outgassing. Consideration must be made to ensure the large thermal masses reach design temperature targets during reflow while not causing an excessive temperature condition on the small thermal mass components due to temperature gradients across the PCB. Because there are so many different types of no-clean solder pastes available, application specific evaluations should be performed to identify if any remaining residue needs to be removed from the boards in final production.

Use of aggressive flux improves solderability yields. When using an aggressive flux, reliability concerns must be taken into consideration. The activators in the flux remove oxides from solder spheres, land patterns, and termination surfaces to promote good solderability during the reflow process. It becomes imperative, however that remaining residues be sufficiently cleaned.

Reflow Profile

Flux has many attributes to facilitate and improve soldering yields. Flux is a chemical agent designed to remove contamination and metal oxides. The job of flux is to protect the solderable surfaces after contamination removal. A common mistake is to use a time/temperature profile that either consumes the flux before the solder melts or does not totally consume the flux due to solder mass, shielding, or low temperature [1]. Ideally, the flux would be consumed just as the solder begins to melt. Activation time should range from 90 to 120 seconds. Flux usually becomes active at around 130°C for tin lead solder pastes. Typically, solder past activation for lead-free solder will be higher, in the 150°C range; however, it is recommended to work with your solder paste supplier for recommendation on that specific solder paste.

Cleaning

The job of the cleaning process is to remove all process residues and render the assembly free of ionic residues. For optimum cleaning of flux residues under the component termination, the solder joints on the perimeter pads should have 75µm or greater standoff height. Package standoff for a BTC is defined as the distance between the land on the bottom of the package substrate and the land on the top of the board surface. Standoff heights are inversely proportional to the land diameters. As land diameters increase, standoff heights decrease. Factors that determine the post-reflow BTC package standoff from the board include the BTC package weight, the volume of solder paste, the land size and land configuration (SMD/NSMD/No-SM).

Electronic cleaning agents must clean the soil, not attack materials of construction; work over an extended time period, be cleaning tool compatible, safe to use in the assembly environment, render no negative impacts to the environment, and cost effective. When cleaning under low profile components, such as QFNs, extended cleaning time is needed to penetrate, wet, dissolve and remove all residues. Contamination trapped under the part, and not totally cleaned can potentially create a reliability concern. The cleaning process must be analyzed to ensure that the cleaning process achieves the reliability standard.

PROBLEM STATEMENT

Highly dense interconnect circuit card designs are populated with greater than 50% bottom terminated components. These miniaturized components are soldered to planar pad surfaces. The standoff gap under these components is commonly less than 50µms (Figure 3). Flux residues can accumulate under the bottom termination (Figure 4). The residue can bridge power and ground connections. The problem is that components, such as QFNs, which have a high solder mass under the component termination are prone to electrochemical migration from residues trapped under the component termination.

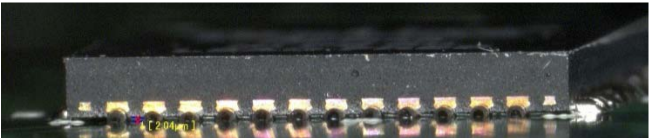


Figure 3: QFN Low Standoff Traps Flux

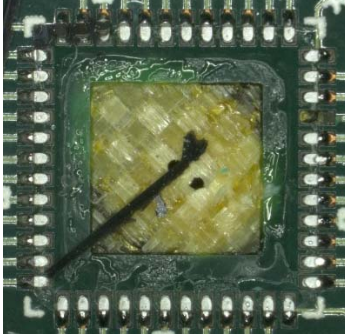


Figure 4: Flux Accumulation under the Bottom Termination

As stated in the introduction, the purpose of this research is to use non-standard QFN test boards with sensors place at both the thermal pads and thermal paddle to measure the activity of a no-clean solder paste flux residue trapped under the bottom termination. The test board has built in design variances at the thermal pad and thermal paddle. The design variances include solder mask definition strategies, pad metallization; solder mask window options, thermal and non-thermal vias, thermal paddle solder deposition and cleaning. Surface Insulation Resistance is the data response used to find the inferences from the research conducted.

QFN TEST BOARD DESIGN

The test board is designed with sensors at both the pad and street areas (Figure 5). Each panel consisted of 3 types of board with variations in thermal paddle configuration. The objective is to correlate reliability expectations with a range of design and process factors. These factors are numerically evaluated using site specific measurements. Design factors built into the test board include variations in surface finish, solder mask definition, thermal vias, solder mask windows, and silk screen dots. Reflow profile, solder pastes and cleaning conditions are process variables within the DOE of this paper. Each of the factors is specifically designed to provide insights into conditions that propagate leakage currents that impact part reliability.

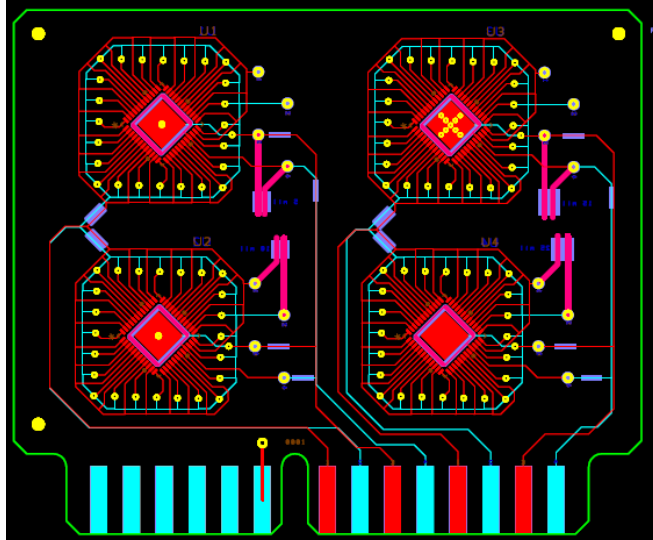


Figure 5: QFN Test Board Design

Board Configuration 9

- Solder Mask Defined vs. No Solder Mask
  - Removal of solder mask increases outgassing channels and should reduce levels of flux trapped under the components post soldering
- No outgassing vias
- Outgassing vias
- No solder mask windows
- Solder mask windows

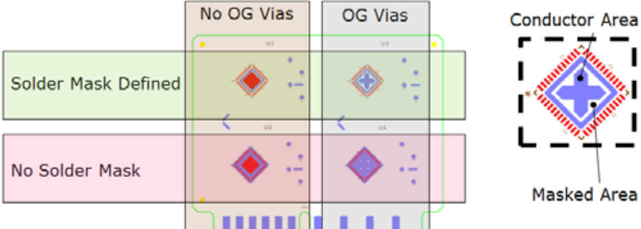


Figure 6: Board 9 layout

Board Configuration 10

- Solder Mask Defined vs. No Solder Mask
  - Removal of solder mask increases outgassing channels and should reduce levels of flux trapped under the components post soldering
- No outgassing vias
- Outgassing vias
- No solder mask windows
- Solder mask windows
- Window Pane Solder Mask Pattern

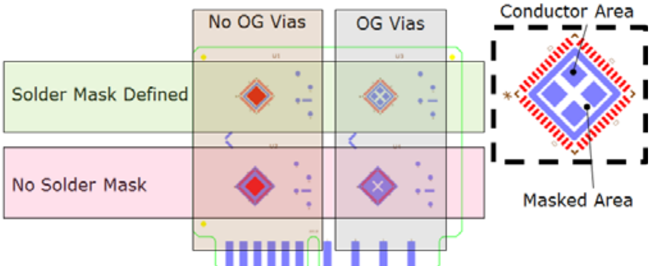


Figure 7: Board 10 layout

Board Configuration 11

- Solder Mask Defined vs. No Solder Mask
  - Removal of solder mask increases outgassing channels and should reduce levels of flux trapped under the components post soldering
- No outgassing vias
- Outgassing vias
- No solder mask windows
- Solder mask windows
- Silk Screen Dots to Increase Standoff Height
  - 25-50µm increase in standoff (Only applied to NSMD configurations)

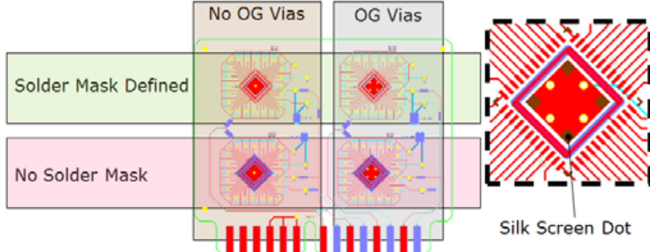


Figure 8: Board 11 layout

EXPERIMENTAL

Factors and Levels Studied

- Test Board Configuration
  - Board 09
  - Board 10
  - Board 11
- Surface Finish
  - OSP Copper
  - Immersion Silver
- Solder Paste
  - Lead-Free No-Clean
  - Lead-Free Water Soluble
- Silk Screen Dots
  - Yes
  - No
- Solder Mask Windows
  - Yes
  - No
- Sensor Looped around Thermal Paddle
  - Yes
  - No
- Cleaning
  - No Cleaning
  - Normal Clean (Some residue remaining under component)
  - Extended Clean (No residue remaining under component)
- Response(s)
  - Component removal by drilling back side of board and using a press to dislodge the component
  - Routing each component off the test vehicle to run site specific ion chromatography
  - SIR @ 40°C, 85%RH, 6 VDC, 300 hour duration, 500kΩ current-limiting series resistor

RESULTS AND DISCUSSION

The results reported and discussed in this paper will focus on the SIR data findings using an industry leading lead-free no-clean solder paste.

The following charts show the failures, warnings, and passed results across all timestamps. The data collected was done over a total of 307 hours with data pulled every day with the exclusion of weekends. The data below will then be used to correlate possible root causes to failures across the -8, -10, -12, and -14 locations. Inferences are made on each board and correlation chart to help explain what exactly is taking place.

Table 1: Timestamp of Resistivity Readings

Timestamp Code	Timestamp
1	6-23-16 at 1030
2	06-27-16 at 1030 (96h)
3	06-28-16 at 1300 (122h)
4	06-28-16 at 1800 (127h)
5	06-29-16 at 1200 (145h)
6	06-30-16 at 1200 (169h)
7	07-01-16 at 1200 (193h)
8	07-05-16 at 0900 (284h)
9	07-06-16 at 0800 (307h)

The site specific resistance readings were taken at the component position. The board has traces connected the perimeter component termination at the unvented test sites (Positions 1 and 2), exposed sensor traces outlining the unvented thermal paddle (Position 3), traces connected to the unvented thermal pads (Position 4), traces connected to the perimeter component terminations at the vented test sites (Positions 5 and 6), exposed sensor traces outlining the vented thermal paddle (Position 7), and traces connected to the vented thermal pads (Position 8).

Table 2 shows the combinations of test points, indicating anode and cathode for each net. Subsequent test results and charts identify each pair of nets being tested by the position A net (Anode).

Table 2: Line Color Designation

Position A (Anode)	Position A Description	Position B (Cathode)	Position B Description
(1)	-8 Unvented Pins – Net 1	(2)	-K Unvented Pins – Net 2
(3)	-10 Unvented Center Lug	(4)	-M Unvented Exposed Trace
(5)	-12 Vented Pins – Net 1	(6)	-P Vented Pins – Net 2
(7)	-14 Vented Center Lug	(8)	-S Vented Exposed Trace

The charts show the breakdown of the nine timestamps divided by the testing locations.

- Points located above the bold green line is higher than 2E9 and is considered a pass
- Points located between the bold green and bold red line is between the range of 2E9 and 1E8 and is considered a warning
- Points located under the bold red line is lower than 1E8 and is considered to be a failure
- Points located at the bottom of the chart are at the lowest recorded value(500K) and have been considered hard failures
- The first twelve boards are No Clean, the following 12 after are Partial Clean and the final 12 are Total Clean

Figure 9 reports failures by test board.

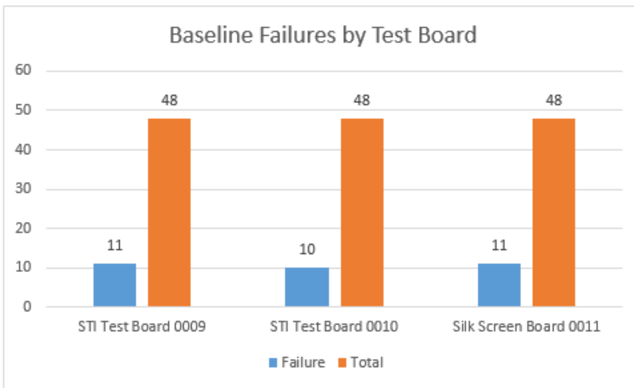


Figure 9: Baseline Timestamp Failure Correlations

No significant correlation between failure rate and the different board types was found.

Figure 10 report failures by surface finish.

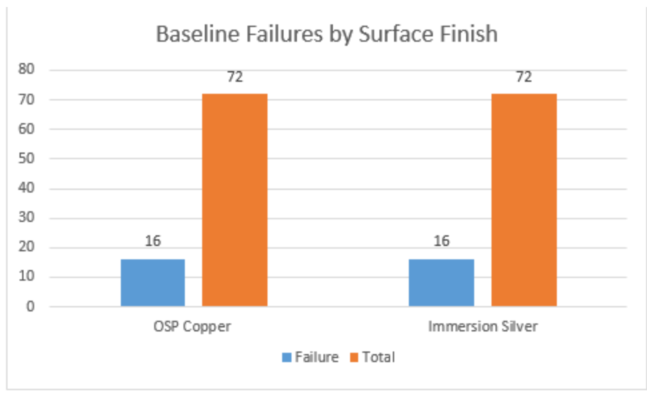


Figure 10: Surface Finish Effects

No significant correlation found between failure rate and surface finish.

Figure 11 reports baseline failures by reflow type.

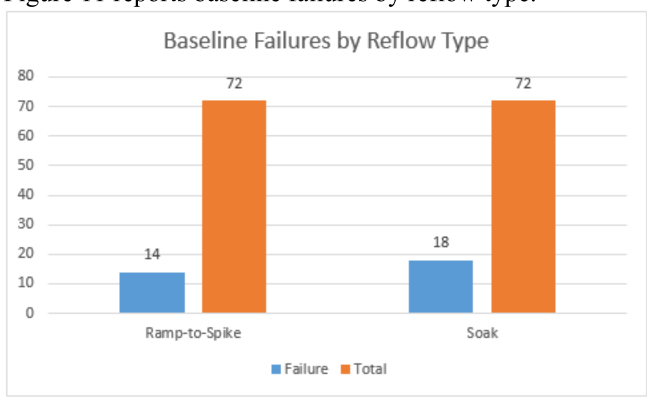
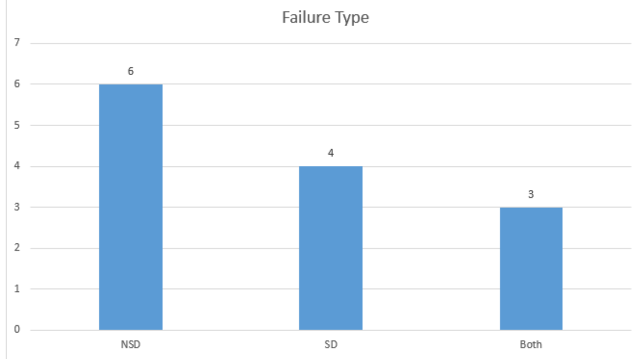


Figure 11: Effects of Reflow on Failure Rate

No significant correlation found from boards reflowed using the Ramp-to-Spike or Soak profiles.

Figure 12 reports the failure by solder mask definition.



NSD: No Solder Mask Definition
SD: Solder Mask Defined
Figure 12: Solder Mask Definition Effect on Failure Type

No significant correlation between failure and the use of solder mask defined or no-solder mask definition.

Figure 13 reports baseline failures by center lug location.

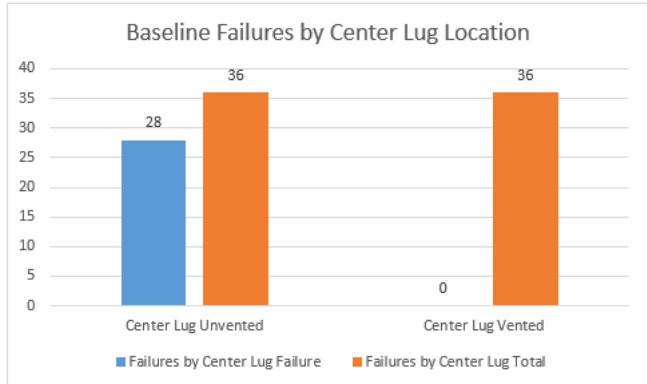


Figure 13: Non-Venting/Venting of Thermal Paddle Area Baseline Failures

Highly significant correlation between Unvented/Vented center lug location and failure rate. With a nearly 78% chance of failure, it is clearly seen that venting the center location will lead to a much higher reduction in failure, even when residue is present. To illustrate the significance of venting the center lug area, the description below illustrates the results of one of the test boards that was not cleaned following reflow.

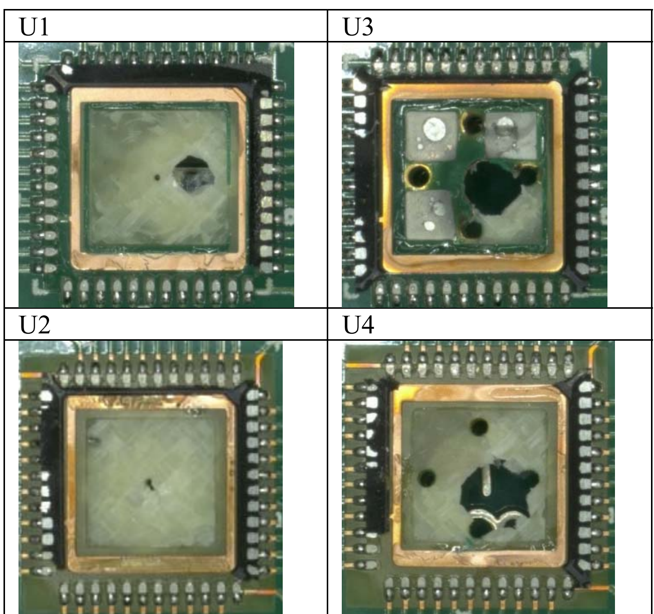
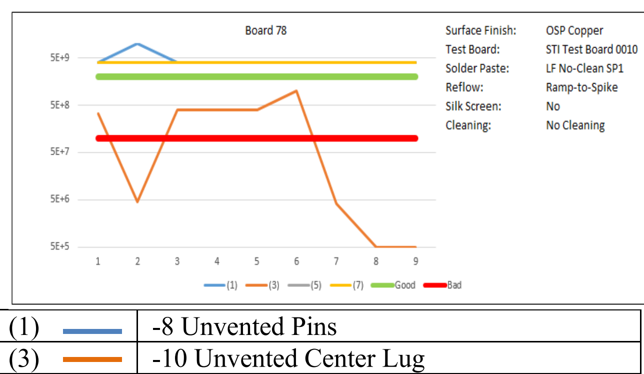


Figure 15: No Cleaning on Test Board 10

Figure 15 images illustrate one of the test boards with components pressed off by drilling a hole from the back side of the board and pressing the components off. The NSMD components tended to have more residue trapped under the component. The level of residue between the non-vented and vented components appeared to be comparable. The limitation of removing the component using a press is the solder at the center lug remained on the component. The benefit of this method is that it allows for seeing residue patterns.

Site specific SIR analysis using the timestamps for collecting the data described in Table 1 was conducted. Figure 16 reports the SIR results. The unvented center lug location dropped initially, moved toward warning, with the unvented component sites moving to complete failure. Flux trapped at the center lug location has no channel to outgas, rendering a high probability of failure. Flux residues at the center lug on the vented component resulted in resistivity levels holding steady without failure. Both the vented and unvented thermal pad areas passed.



(1)	blue line	-8 Unvented Pins
(3)	orange line	-10 Unvented Center Lug
(5)	gray line	-12 Vented Pins
(7)	yellow line	-14 Vented Center Lug

Figure 16: Timestamp of SIR data for Board 78

The objective for boards partially cleaned was to leave some residue under the bottom termination center lug area. The thermal pads were mostly clean. Figure 17 illustrates the four component sites for one of the partially cleaned boards.

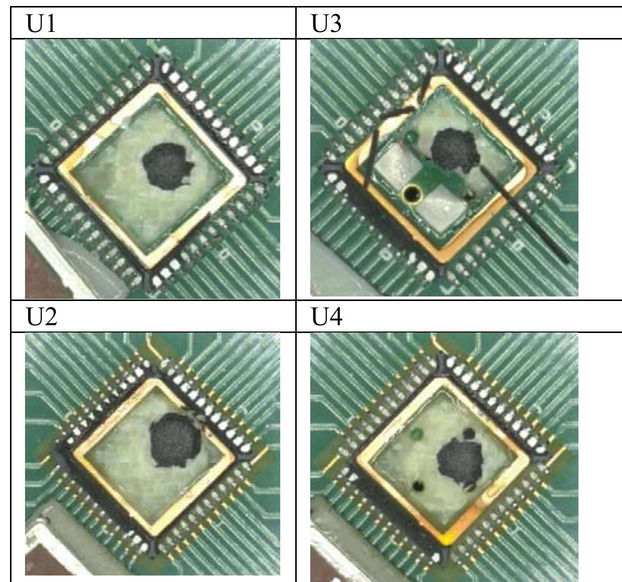
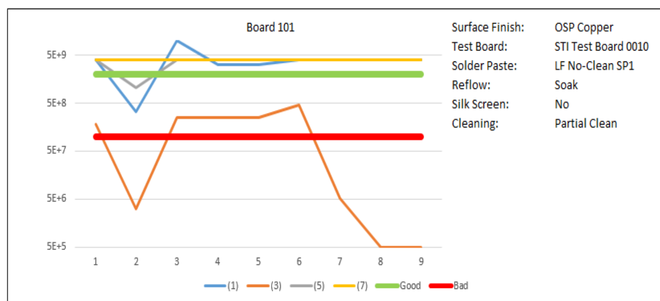


Figure 17: Partially Cleaned Board Images



(1)	blue line	-8 Unvented Pins
(3)	orange line	-10 Unvented Center Lug
(5)	gray line	-12 Vented Pins
(7)	yellow line	-14 Vented Center Lug

Figure 18: Timestamp of SIR data for Board 101

Similar to the Non-Cleaned test board example, the unvented center lug components saw a resistivity drop initially, moved toward warning, with the unvented component sites moving to complete failure. This test finding further indicates that residue trapped at the center lug on a non-vented component is still active and has a high probability of failure.

Figure 19 reports the failures by pin location.

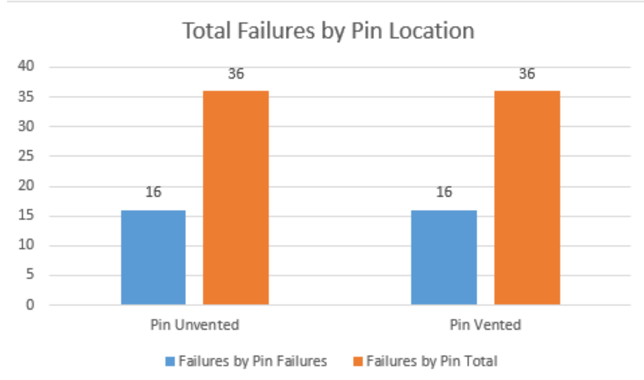


Figure 19: Thermal Pad Failure on Vented and Unvented Components

No significant correlation between Unvented and Vented Pin locations and failure rate was found. Venting the pin region does not appear to impact the resistivity of residues at thermal paddle. Solder mask definition images show that a Non Solder Mask defined component has more residue at the pin location than does a No-Solder Mask defined component. Figure 20 is a Non-Solder Mask defined board not cleaned. Flux residue tends to bridge most thermal pads. Figure 21 is a No-Solder Mask defined board not cleaned. The images show less residue bridging thermal pads. We believe this is due to increased standoff gaps, which improves flux outgassing. The data on NSMD and No Solder Mask definitions was inclusive. Further study in this area is needed for failure tendencies at the Thermal Pads.

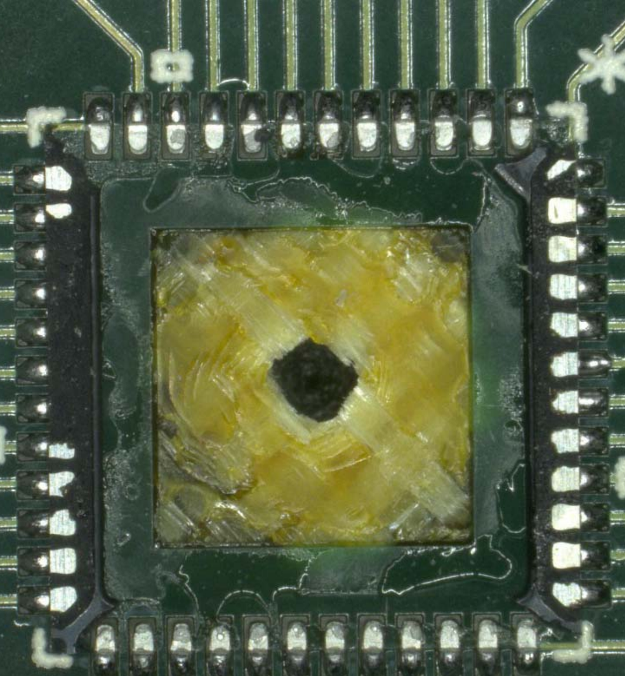


Figure 20: NSMD Residue Example at Thermal Pad Area

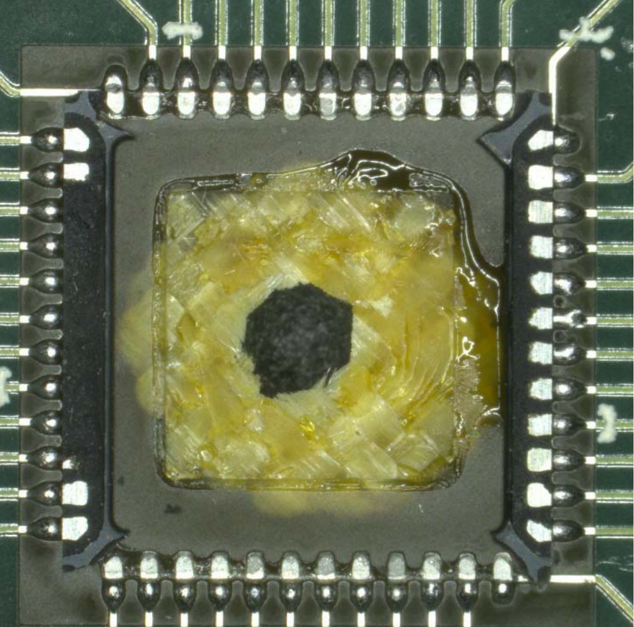


Figure 21: No Solder Mask defined Residue Example at Thermal Pad Area

Figure 22 reports the failures by cleaning process.

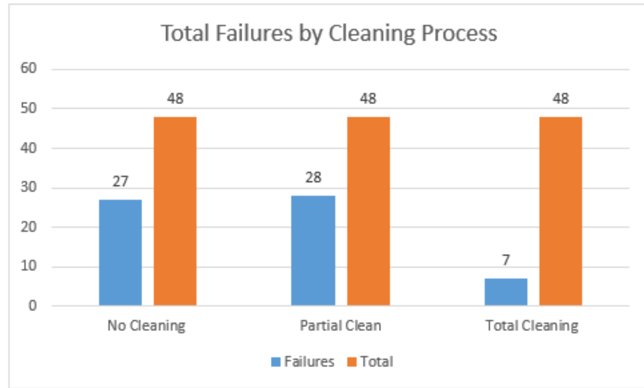


Figure 22: Cleaning Effects on Failure

The data infers a highly significant correlation between cleaning process and failure rate. There was no noticeable difference between No Cleaning and Partial Clean data findings. There were a few failures noted on Total Cleaned boards. This can be explained by residue formation noted when removing components on the Total Clean boards. When removing components, on some Total Clean boards, small pockets of residue was still present.

Figure 23 is Test Board 10 with very minimal visible residue. There is some residue seen on U3 vented component. On U1, U2, & U4 components very little visible residue is seen. The SIR time stamp for this parts finds no failure (Figure 24).

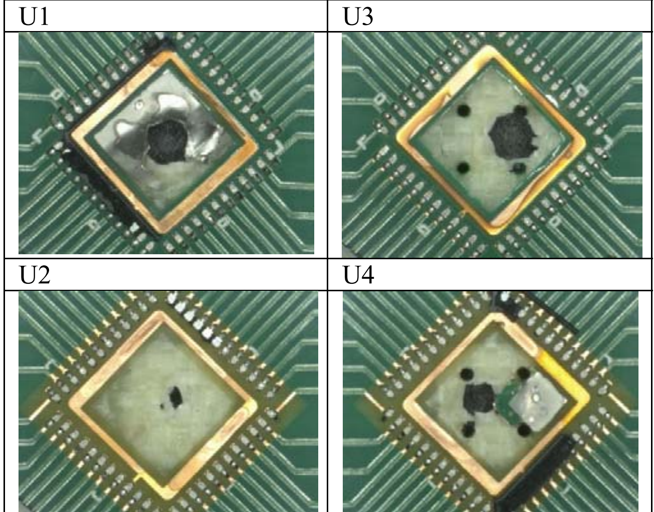
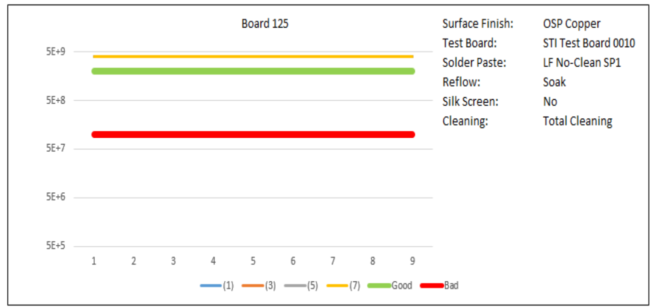


Figure 23: Total Clean Board Images



(1)	blue line	-8 Unvented Pins
(3)	orange line	-10 Unvented Center Lug
(5)	gray line	-12 Vented Pins
(7)	yellow line	-14 Vented Center Lug

Figure 24: Time Stamp of SIR data for Board 125

On a Totally Clean board that still has some residue left under the component there is the potential for an intermittent failed part. These failures are propagated by small pockets of residue still remaining under the part. Figure 25 illustrates a small level of residue bridging the center lug and thermal pads. This residue was sufficient to cause leakage.

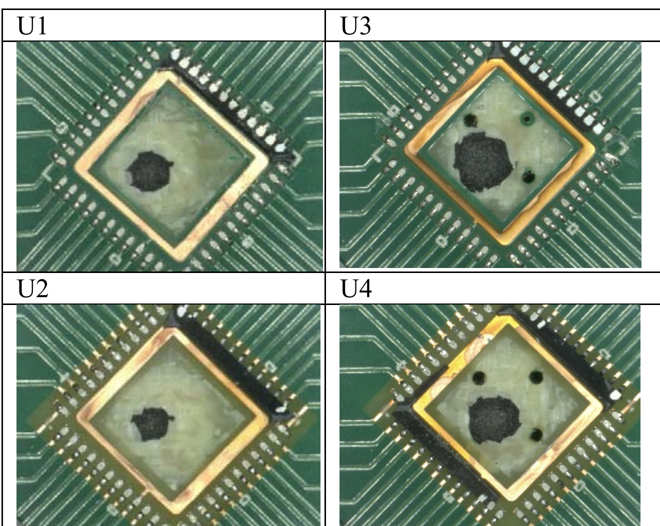
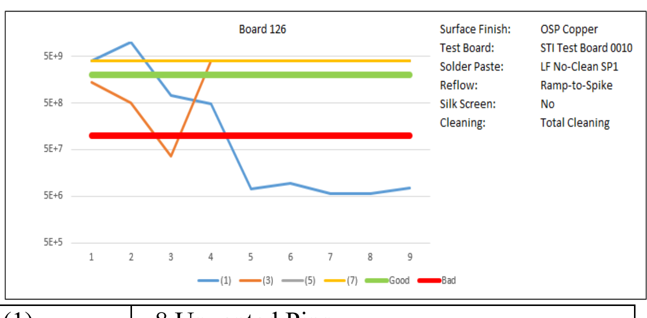


Figure 25: Small Level of Residue Bridging the Center Lug and Thermal Pads on U1



(1)	-8 Unvented Pins
(3)	-10 Unvented Center Lug
(5)	-12 Vented Pins
(7)	-14 Vented Center Lug

Figure 26: Leakage at the Unvented Pins and Unvented Center Lug on a Total Cleaned Board

CONCLUSIONS

The focus of this paper was to build an understanding of flux residue entrapment and its potential to cause leakage currents under QFN components. QFN components have inherent challenges due to the large thermal mass of solder under the component termination, low standoff gaps and entrapment of heavy flux residue deposits. The non-standard site specific test vehicle provided the ability to study the effects of flux residue under the bottom termination and other key factors such as solder mask definition, reflow profiles, ground lug designs and cleaning effects.

Inferences from the data findings found that the driving factor for failure is absence of vent holes for solder flux residues to outgas at the center ground lug. When vent holes where placed in the center ground lug, residues could be present but did not cause failures. One could infer from these findings that when no-clean flux has a channel to outgas, the activity of the trapped level is less problematic. When flux residues do not have a channel to outgas, entrapped residues are active in nature and have a high potential to form leakage currents when the part is exposed to humid and moist conditions.

The data also indicates that improper cleaning can be problematic. Removal of flux residues under a low standoff part is high challenging. Longer wash time and pressure is needed to dissolve flux residues, create a flow pattern and totally clean under the component termination. When residues are totally cleaned, the risk of leakage currents is significantly reduced. Conversely, when residues are still present after cleaning, leakage current risks are elevated on components that did not have the vented thermal paddle.

The non-standard test vehicle design is an effective method for understanding residue effects and design options for developing a risk profile. The data findings can be used to optimize and develop best case conditions for improving the reliability of bottom terminated components assembled on printed circuit boards.

FOLLOW ON RESEARCH

The DOE used for conducting this research study only reported findings for the no-clean solder paste using SIR responses. The data findings for the water soluble solder paste was not reported. Additionally, the site specific Ion Chromatography analyses was not reported. Follow on research papers will report these data findings and measure their significance.

This research provided significant insights into the thermal paddle design options for improving reliability when flux residues are trapped under the component termination. Further work in determining optimal design rules will for the thermal paddle area is needed. The insights learned from this research study will be valuable in guiding follow on research to develop best practices for improving reliability.

Follow on research is needed to determine design options for increasing standoff gaps. The research continues to point to the benefits of increasing standoff gaps. By increasing standoff gaps, the levels of flux residues trapped under the bottom termination will be reduced. Additionally, the flux has an improved channel for outgassing.

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