

APPLICATION OF YOUNG-LAPLACE EQUATION REVEALS NEW POSSIBILITIES FOR THERMAL PAD DESIGN

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ABSTRACT

Driven by miniaturization and increasing power dissipation there is a strong need for better cooling of electronic components on printed circuit boards (PCB). One major contributor to the thermal resistance is the PCB itself. In IPC-7093 several thermal via configurations are discussed which enable the cooling of bottom terminated components through the PCB. The main risk of the designs is always the wicking of solder into the vias and the protrusion of solder on the opposite side of the PCBA. All suggested measures to avoid those risks are either not cost neutral (e.g. plugging) or thermally not optimized (e.g. solder mask). In this paper it will be shown how the application of the Young-Laplace equation $\Delta p = \gamma \mathcal{H}$ can lead to a thorough understanding of the soldering process of exposed pads (ePads) and heat slugs.

The use of via arrays without solder mask or plugging is suggested. It will be shown that solder wicking can be completely avoided by using an optimized land-pattern design. Due to conflicting targets the formation of solder protrusions can't be completely suppressed - though reduced down to a ppm-level. A slight modification of the electronic packages themselves will be proposed which is able to resolve this conflict.

With this technology thermal conductivities of up to $11700 \frac{W}{K m^2}$ can be achieved.

For an ePad with dimensions 8mm x 8mm this would result in an R_{Th} of the PCB of only $1.33 \frac{K}{W}$.

Key words: ePad, Modification, Grooves, Wicking, Protrusion, Thermal Conductivity

INTRODUCTION

Today's electronic devices mainly consist of printed circuit board assemblies (PCBAs), where the printed circuit board (PCB) itself has the functions of conducting electric currents and isolating electrical potentials on the one hand and to spread the heat dissipated within components on the other hand. Electronic components with high power dissipation often feature a heat slug or an exposed pad (ePad) intended to be soldered to an extended land area to enable efficient cooling through the PCB (see Figure 1). As shown in Figure 2 the thermal conductivity through the PCB is one major contributor to the overall thermal conductivity and depends significantly on the size (hole diameter) and density (pitch)

of plated through holes placed within the ePad area (cf. Figure 3).

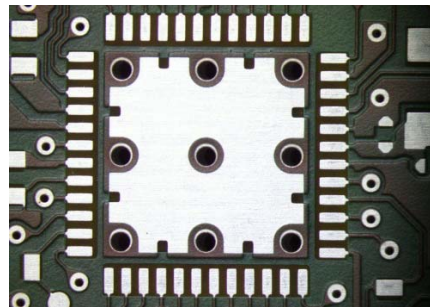


Figure 1: Image of a PCB with exposed pad soldering area for a QFN component.

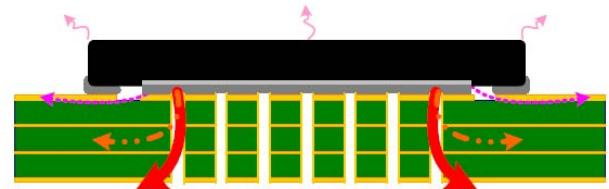


Figure 2: Heat conduction paths for an electronic component, here a quad-flat no lead package, soldered onto a PCB thermal pad (taken from [1] with permission): Heat can be transferred by convection, by spreading laterally in the PCB and by conduction along plated through holes (PTHs).

Guidelines for choosing among possible PCB design options at the exposed pad can be found in IPC-7093 [2], a recent comprehensive review and appraisal of different design options is given in [3] (see also references therein and Figure 4).

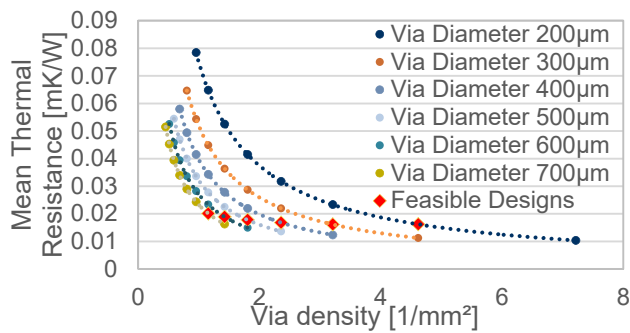


Figure 3: Depending on the ePad design the mean thermal resistance of the PCB can vary between $0,1 \frac{mK}{W}$ and $0,015 \frac{mK}{W}$.

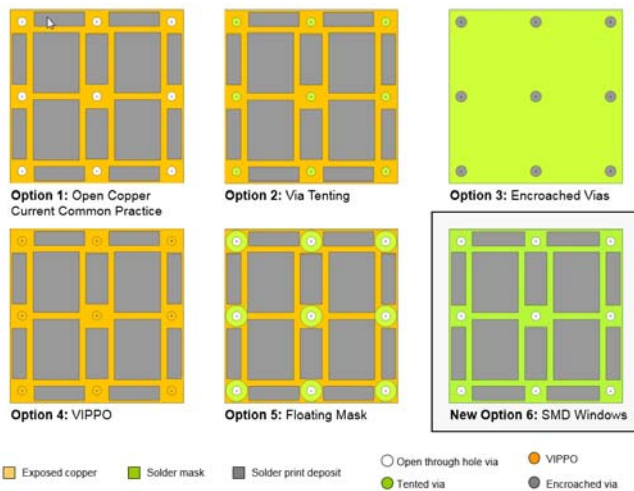


Figure 4: PCB thermal pad design options (taken from [3] with permission).

Besides an optimized thermal conductivity a very low failure rate during production is also of major importance. Today's industry standard is to aim for a Six-Sigma (6σ) Process with a short term Cpk of 2 resulting in long term failure rates during production below 3.4 ppm. In order to assess whether a process is 6σ capable it is necessary to measure or describe the relevant process parameter including its characteristic distribution and to define a lower and/or upper threshold for a failure. Neglecting non-wetting (termination-related failures) and reflow shifting (avoidable by design) for ePad solder joints only two relevant failure mechanisms are known: (i) Wicking of solder into (open, unplugged) thermal vias leaving a too large area of the slug unsoldered; (ii) Formation of protrusions of solder on the opposite side of the PCB (see Figure 5, where (i) is indicated by the area underneath the components ePad in red color and (ii) is indicated by the protrusion of solder marked with gray color on the bottom side of the PCB).

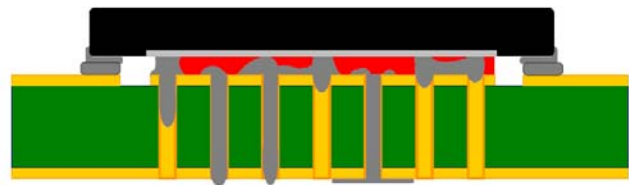


Figure 5: Common failure modes related to the use of open plated-through holes for ePad soldering: solder wicking and formation of solder protrusions (taken from [1] with permission).

The various thermal pad design options all have certain advantages and disadvantages with respect to thermal conductivity and cost, and these factors have to be balanced against the failure propensity for the above described failure modes:

(a) Whereas designs involving tenting or plugging of vias avoid solder wicking, these are usually not cost-neutral. If vias are covered with e.g. solder mask this may also have a negative impact on thermal performance.

(b) Designs separating the vias from the solderable PCB areas using solder-resist barriers obviously involve restrictions on the density of PTHs and thus have a negative impact on the overall thermal conductivity.

Moreover, spill-over of solder into vias can occur for dense designs with only narrow resist barriers, so that wicking and/or protrusions can occur.

The present manuscript will focus on the maximization of thermal conductivity through the PCB by using open Cu with plated through holes (PTH) in a dense array (option 1 in Figure 4). It will be shown that the occurrence of both failure modes, solder wicking and solder protrusions, can be thoroughly understood by application of the Young-Laplace equation and can be completely avoided by appropriate knowledge-driven design.

MODELLS FOR SMT PROCESS

Young-Laplace-Equation

The Young-Laplace-Equation $\Delta p = 2\gamma H$ describes how the surface tension γ of a medium together with the curvature H of the mediums interface (e.g. solder to air) results in a pressure Δp on the medium. Using the two local radii R_{\perp} and R_{\parallel} which define the curvature in every point of the surface the Young-Laplace equation can be written as $\Delta p = \gamma \left(\frac{1}{R_{\perp}} + \frac{1}{R_{\parallel}} \right)$. The equation applies for liquid media in general – liquid solder being no exception. Since liquid solder has a dynamic viscosity close to water dynamic effects can be mostly neglected. (See Figure 6) [4] [5]

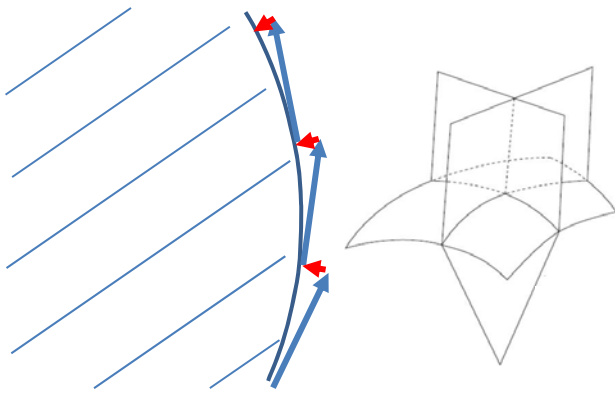


Figure 6: Schematic drawing of the correlation between the surface tension (blue) and the internal pressure (red) due to a curved surface. Schematic drawing of local radii (taken from [6]).

Solder Wicking

Solder wicking can be completely understood by application of the Young-Laplace equation to the geometry of the ePad solder joint (see Figure 7). In general wicking of solder into vias is only possible if solder has contact to the vias and the capillary pressure Δp_{Via} of the vias is lower than the pressure Δp_{Comp} due to the capillary between PCB and component.

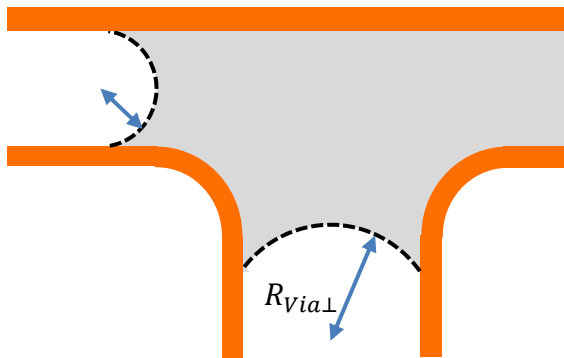


Figure 7: Schematic Cross Section of an ePad solder joint. Due to the fixed wetting angles the radii of the fillets are purely geometry dependent.

For simplicity let us assume that both the terminations of the PCB and the component have the same wetting angle θ for solder. With this assumption local radii of a solder joint between PCB and component are $R_{Comp\perp} = -\frac{1}{2} h \cos \theta$ and $R_{Comp\parallel} \approx \infty$ (i.e. we neglect the curvature resulting from the finite lateral size of the solder joint). The local radii of the solder surface inside a via are $R_{Via\perp} = R_{Via\parallel} = -R_{Via} \cos \theta$. As a result $\Delta p_{Comp} = -2\gamma \cos \theta \frac{1}{h_{standoff}}$ is always smaller than $\Delta p_{Via} = -2\gamma \cos \theta \frac{1}{R_{Via}}$ as long as the radius of the via R_{Via} is bigger than the standoff h . Since for

electronic components typical standoffs do not exceed $150\mu\text{m}$ it is safe to assume that vias with a radius larger than $150\mu\text{m}$ will not exhibit solder wicking. It is strongly recommended to implement this design rule in IPC-7093. [2]

Solder Protrusion

How solder protrusions (see Figure 8 for an example) are formed is not fully understood. What is known is that they only occur for vias with at least a partial solder filling. The solder then is pushed out of the via due to formation of large volumes of gas which could either result from outgassing of flux trapped in the via or by outgassing of the PCB base material through so called plating voids in the via walls during the reflow process (cf. Figure 9).

Since in case of a solder protrusion the local radii R_{\perp} and R_{\parallel} are obviously different from those in the surrounding vias the pressure in those vias is much higher. Solder protrusions only occur if the flow of solder and gas into neighboring vias is restricted by capillary friction or other dynamic effects. The most effective way to avoid solder protrusions is to prevent solder from entering into the vias altogether.

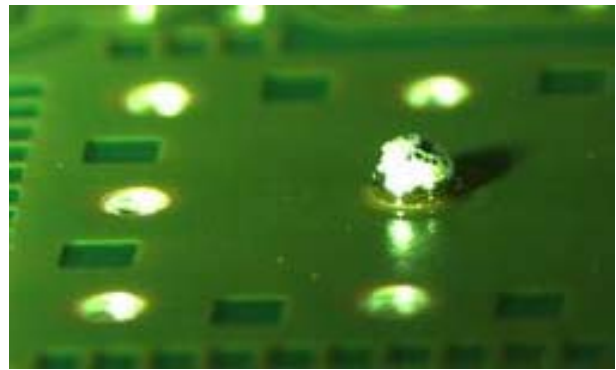


Figure 8: Microscope picture of solder protrusion under a QFN ePad.

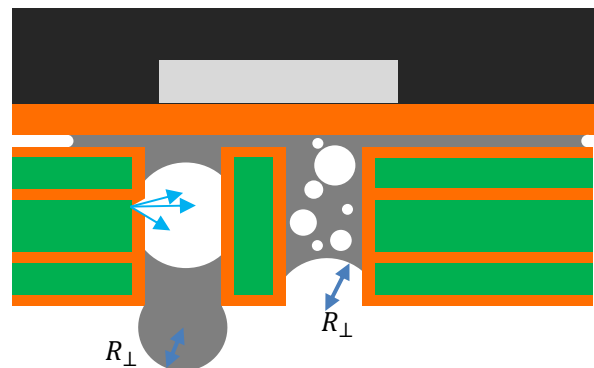


Figure 9: Schematic cross section of an ePad solder joint exhibiting a solder protrusion. Voiding caused by outgassing plating voids (left via) and outgassing flux (right via).

It has to be assessed how much solder (volume V) has to be applied for an ePad solder joint to enable a sufficient soldered area A on the one hand and no excess solder in the vias on the other hand. For a component with nominal component standoff h and ePad area A_{Max} this can be calculated as $V_{Max} = A_{Max} h$. Since most ePads are sufficiently large edge effects can be neglected in this equation.

Obviously the optimum solder joint is formed if the complete solderable area A_{Max} is soldered and the filling f of the vias is zero (cf. Figure 10). Due to scattering of the component standoff h , the printed solder volume V and the solder resist it is not possible to always achieve this optimum. Typical measures to avoid a situation with solder in the vias (11a) would be a reduction of solder paste (11b) or the usage of solder resist around the vias (11c), both resulting in a great reduction of soldered area and significant restriction for the density of the via placement (cf. Figure 11). We propose an alternative solution which provides significant buffer volume to accommodate for the scattering without any loss of solderable area (11d). This can be achieved by a small modification of the components – solder reservoir grooves.

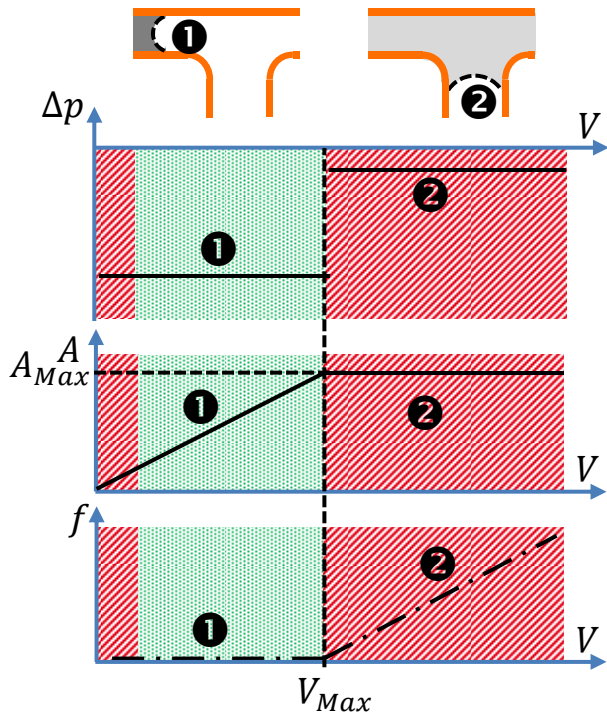


Figure 10: Graph of internal pressure Δp , soldered area A and filling of vias f . An optimal design is achieved if the solder volume V_{Max} is applied.

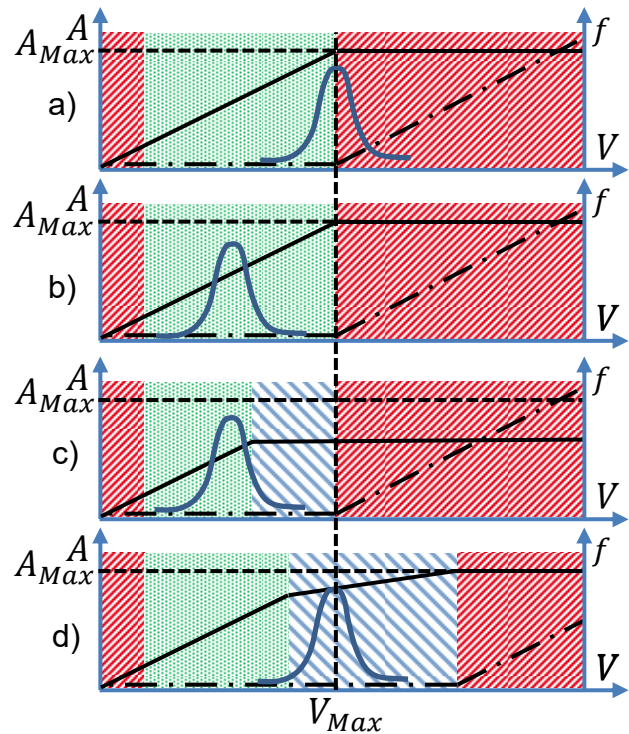


Figure 11: a) Process scattering (blue Gaussian curve) results in filled vias if the nominal solder volume is set to V_{max} . This can be avoided by b) reduction of the nominal solder volume, c) application of solder resist. d) Solder reservoir grooves provide a large buffer volume without reducing the solderable area.

SOLDER RESERVOIR GROOVES

Design

The use of grooves, cuts, dimples & holes in electronic components has become more and more common over the last years. Most of the modifications are designed to make the package optically inspectable, but also grooves to stop mold flow or to enhance mold adhesion are not uncommon. The proposed modification are grooves at the bottom side of the ePad which work as a buffer volume for excessive solder preventing it from flowing into thermal vias (see Figure 12). In principle it is possible to saw, punch, mill or drill the structures, but etching is clearly the preferred technology.

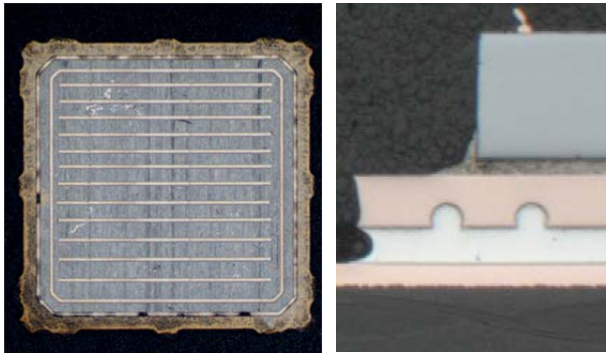


Figure 12. Visualization of QFP ePad with etched solder reservoir grooves. Cross section of soldered grooves.

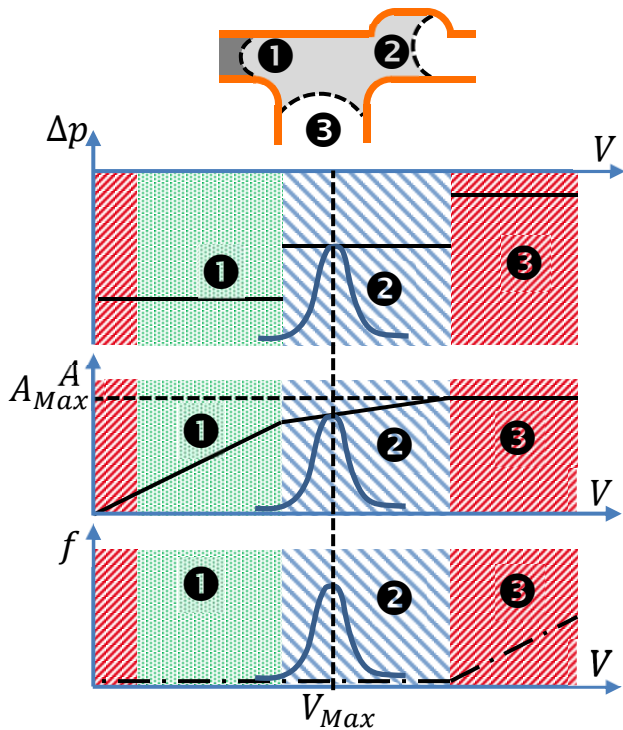


Figure 13. Graph of internal pressure Δp , soldered area A and filling of vias f for an ePad with solder reservoir grooves. The pressure of the component standoff is lower than the pressure of the grooves which is still lower than the pressure of the vias.

Working principle

In order to understand why the grooves work and how they should be designed it is necessary to apply the Young-Laplace-equation $\Delta p = \gamma \left(\frac{1}{R_L} + \frac{1}{R_H} \right)$ once more.

The goal is that the solder is filling the component standoff, is then buffered in the grooves and will only fill the vias if this buffer overflows. Therefore the capillary pressure Δp of the grooves should be between the capillary pressure of the component standoff and the capillary pressure of the vias. The width w of the grooves should be at least two times the maximum component standoff, but still well below the

diameter of the thermal vias. The depth d of the grooves should be as deep as possible in order to generate sufficient buffer volume (cf. Figure 13). Depths below $100\mu\text{m}$ are not recommended. To accommodate for all scattering parameters it is recommended that the buffer volume is as big as the nominal solder volume.

Arrangement of thermal vias

Since solder resist below the ePad is no longer necessary the proposed design enables a high degree of freedom for the placement of thermal vias. Vias can be placed directly below the die enabling optimized thermal paths (see Figure 14 for an example).

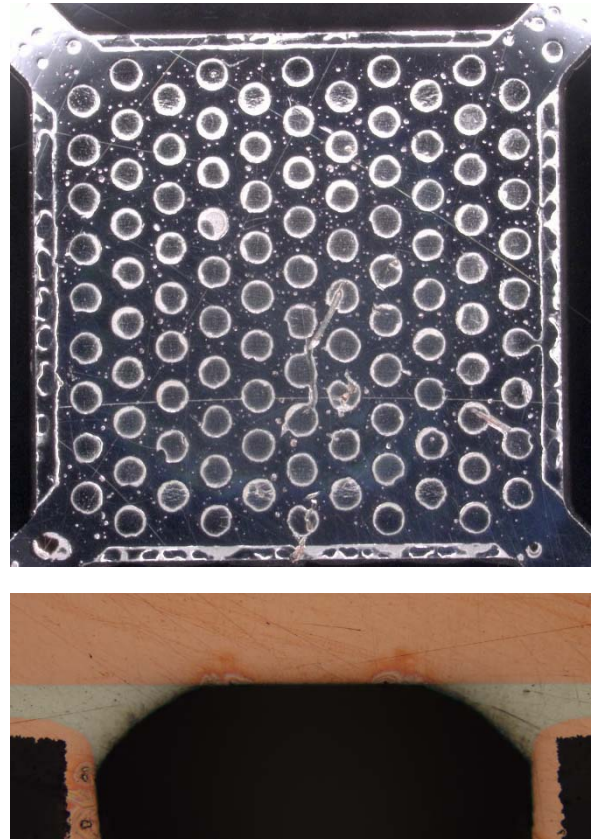


Figure 14. Flat Section and Cross Section of ePad solder joint with hexagonally closed packed via array. All surfaces are completely soldered. Vias are not filled with solder.

In case of components with high power consumption it is sometimes necessary to use ePads with very low R_{Th} through the PCB. Using vias with a diameter of $500\mu\text{m}$ in a hexagonally closed packed array with pitch 1.0mm results in thermal conductivities per area of more than $36 \frac{W}{m K}$. For an ePad with dimensions $8\text{mm} \times 8\text{mm}$ this would result in an R_{Th} through the PCB of only $0.69 \frac{K}{W}$. Besides the significantly reduced scrap rates this could become a strong driver for the new design.

CONCLUSION

It has been shown that for ePads the failure modes solder wicking and solder protrusion, which can occur with failure rates of up to several percent, can be completely avoided by intelligent pad and component design. The radius of the thermal vias R_{via} should always be bigger than the maximum acceptable component standoff h . In order to avoid the formation of solder protrusions buffer volume for excess solder has to be created. The best way to do so is to use components with groove structures at the bottom of the ePad. In order to avoid solder wicking into the grooves the width of the grooves should be at least two times the maximum component standoff, but still well below the diameter of the thermal vias.

This design enables a high degree of freedom for the placement of thermal vias. Due to the dense packing of vias mean thermal conductivities through the PCB of up to $62 \frac{W}{m.K}$ can be achieved. This could open up new possibilities for components with high power consumption which up till now had to use expensive technologies such as inlays, plugged vias, etc...[3]

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