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3D IC INTEGRATION TECHNOLOGY DEVELOPMENT IN CHINA

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ABSTRACT
China's semiconductor foundry and microelectronic packaging industries are embracing the move to join 3D IC integration technology development with ample funding and rapid pace. An overview of the recent progress on the efforts in 3D IC integration technology development by the leading domestic companies and research institutes is provided here.

Because China still lacks in infrastructure for advanced and modern front end of the line (FEOL), backend of the line (BEOL), and middle-end of the line (MEOL) process capabilities for 300mm wafers, development efforts on 3D IC integration have many limitations to begin with. The efforts adopted by some leading research institutes and back-end packaging assembly and test companies; however, appear to be quite ingenuous and pragmatic, by selecting more easier "cutting-in" research projects and processes that require less initial capital investment and infrastructural establishments.

The pattern of latest development efforts can be divided into two major areas: 1) TSV materials, processing, and interconnection; 2) low-cost interposer and 2.5D integration assembly application in wafer level CSP packages for MEMS and sensors using small-sized wafers. The short term perspectives and longer term growth opportunities for China's indigenous development efforts on 3D IC integration is summarized in conclusion.

Key words: TSV, 3D IC Integration, Interposer

INTRODUCTION

China Semiconductor Industry

Before we discuss the red-hot topic of 3D IC integration technology, it is very helpful to review some background information and update on the status of China's semiconductor and back-end packaging assembly industry; how the industry's growth had been planned and cultivated to arrive at the present condition. Having established such bases of knowledge, it will then be much easier to understand and follow the approaches that the semiconductor and microelectronics assembly industries in China are taking to "catch up" with the 3D IC and TSV integration technologies.

In recent years (2010/2011), China purchased over 40% of world's semiconductor ICs worth more than $100 billion for use in electronic products and systems. Yet, ironically, less than five percent of these ICs were made locally by domestic manufacturers. There is, therefore, a large IC consumption/production gap that amounted to $87 billion in 2010 for China [1]. In fact, as of mid-2012, none of the top 20 of world's semiconductors suppliers (including foundries) is Chinese. For the record, the top 10 semiconductor suppliers for 1H2012 according to IC Insights [2] are shown in Table 1. Four countries contributed to the first nine suppliers: USA, Korea, Japan, and the Republic of China (Taiwan). China's top four semiconductor foundries--SMIC, Grace Semiconductor, HHNEC, and HLMC are not even on the list for the next 10 rankings. Furthermore, according to a recent forecast by SEMI on the 2013 semiconductor materials global market share [3], shown in Figure 1, China's share (as part of the "Rest of Asia" group of 12%) will be substantially behind its neighbors such as the Republic of China, Japan, and Korea. Per DigiTimes Research, the total China IC foundry industry output is estimated to be $3.29 billion for 2012 [4].

Table 1. Top Semiconductor Suppliers in 1H2012

Company	Country	Rank
Intel	USA	1
Samsung	Korea	2
TSMC	ROC (Taiwan)	3
TI	USA	4
Qualcomm	USA	5
Toshiba	Japan	6
Renesas	Japan	7
SK Hynix	Korea	8
Micron	USA	9
ST Microelectronics	Netherlands	10

Source: IC Insights McLean Report, Aug. 2012

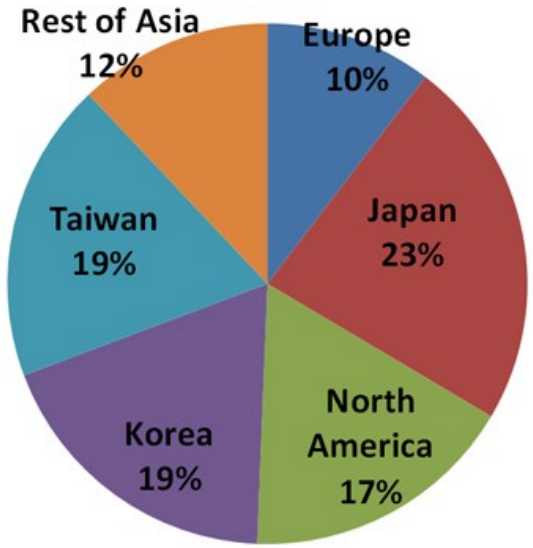

Figure 1 Global Market Share of Fab Materials (SEMI)

Because of this huge IC consumption/production deficit suffered by China and the relatively small scale of China's semiconductor suppliers, for over a decade, the Chinese government and its domestic semiconductor industry have been trying very hard to increase the capability in IC design and production capacity for silicon wafer fabs in order to remedy this situation. The most recent 12-5 Plan (12th Five-year plan for 2011-2015) has eight focal industries for major upgrade and funding. These industries are:

1. IT and electronics manufacturing
2. Steel
3. Automotive
4. Biotechnology
5. Machine manufacturing
6. Rare earth materials
7. Concrete materials
8. Aluminum industry

For high-end manufacturing, semiconductor and IT are of course selected as the key focal industries for funding to encourage growth and expansion of indigenous, homegrown semiconductor wafer fabs and back-end assembly industries. However, for many years, the barriers that have been hindering China's advance in semiconductor technology know-how and growth still existed:

- IC design capability—China still lags behind the Western and Japanese/Korean players in designing sophisticated, advanced ICs based on leading-edge process nodes such as 30nm and below. Such highly proprietary IP knowledge and experience cannot be gained overnight. Foreign players typically have prohibited the transfer or sales of advanced, leading-edge design and processing technology to China.
- Insufficient availability of talents of experienced engineers and technical personnel to carry out leading-edge research and development; domestic companies often rely on technology collaboration with foreign players.

To remedy this situation, China government has implemented the "863 Project" on high-value, high-end advanced technologies that fund projects to research institutes and the industry to focus on research and development of next-generation technology platforms such as Internet of Things and Cloud Computing. Local companies are also more aggressive in requesting foreign partners to share or transfer their advanced IP and know-how in joint-venture investments. When the 3D IC integration using TSV technology came along in recent years, China sees it as a perfect opportunity and platform to further advance its semiconductor and backend packaging assembly industries.

China Semiconductor Foundries

Silicon wafer based CMOS technology form the largest segment in China semiconductor industry. The larger fabs and foundries, including SMIC, Grace Semi, HHNEC, and HeJian all have capabilities for processing 300mm wafers. However, there are also many smaller fabs focusing on other types of semiconductor, such as MEMS, III-V semiconductors, LED (light emitting diode), sensors and optoelectronics. In 2011, China already had 68 LED wafer fab companies. These types of fabs may use non-silicon wafers such as GAN and GaAs wafers. For example, the company CSMC still processes 150mm wafers for MEMS. Total investment spending in China for 2012, as shown in Table 2 [5], is catching up with EU and Japan.

Table 2. Global Semiconductor Industry Spending (K$)

	2011	2012	
Americas	8944	6158	
China	3126	2934	
EU/Mideast	3767	3041	
Japan	5525	3825	
Korea	7400	10255	
SE Asia	2471	1792	
Taiwan	7997	7048	
Total	39230	35053	

(SEMI "World Fab Forecast" Nov 2011) [4]

CHINA 3D IC TECHNOLOGY STATUS

The approaches taken by many of the domestic institutes and companies to pursue the 3D IC integration are similar: aiming at efforts that require less initial extensive capital investments and lower technical barriers. With plenty of funding, many companies started such approaches to initiate TSV and 3D stacking/wafer level packaging technology without extensive scope or broad objectives. Thus, while in other regions of the world, modern advanced 3D IC integration using TSV are aimed at applications for high performance memory on logic, high performance CPU and GPU and other ASIC chips as the "mainstream" focus, the approaches taken by China are

somewhat different, with beginning emphases on low cost TSV and 3D stacking applied to MEMS, sensors, and camera modules.

3D IC Research Topics

At the August, 2012 ICEPT in Quilin, China's premier packaging conference, no less than forty papers dealt with 3D IC integration and through silicon via (TSV). Considering that TSV and 3D stacking is still in an embryonic development stage for China's backend manufacturing industry, such pace of progress is indeed quite impressive. By reviewing the relevant reports given in this conference, a quick glimpse of the development efforts undertaken by the leading institutes may be revealed. Table 3 lists the four topics of interest: TSV process and materials; wafer thinning, handing, and bonding; silicon and glass interposer for 2.5D integration; and 3D packaging and applications. For each technical field, the contributing institutes and companies are listed.

Table 3. Summary of Topics and Contributors

Research Topics	Technical Field	Institute/Company
TSV	Wet etching	SIMIT-CAS
	Copper plating	Peking Univ, Huazhong Univ. Tsinghua Univ.
	Stress analysis	IME-CAS, Fudan
	Modeling/test	Xidian Univ. BUT
Wafer Handling	CMP process	Tsinghua Univ.
	Carrier-less	Huazhong Univ.
	Low temperature bond	SIMIT-CAS
	Glass bonding	Peking Univ.
Interposer	Glass TGV	IME-CAS
	Micro bumping	Shanghai JiaoTong
	Silicon interposer	BUT
Packaging	Wafer level package	JCAP Co., Fudan Univ., Peking U.
	LED	Shanghai Univ.
	MEMS	Guilin Univ.
	Sensors	Peking Univ.
	Optical	IME-CAS

(**Note:** SIMIT=Shanghai Institute of Microsystem and Information Technology, CAS=Chinese Academy of Sciences. IME=Institute of Microelectronics, BUT= Beijing University of Technology, JCAP= Jiangyin Changdian Advanced Packaging Co.)

It can be said that the major 3D IC integration technology development efforts are spear-headed by CAS--the Chinese Academy of Sciences and some of the major State Key Laboratories. Within CAS, the two largest research organizations are the Institute of Microelectronics (IME) in Beijing and the Shanghai Institute of Microsystems and Information Technology (SIMIT). Top notch universities such as Tsinghua University, Peking University, Shanghai JiaoTong University, Fudan University, and Huazhong University all have research projects relating to 3D TSV, interposers, and 3D WLP packaging applications. In the following section, detailed research reports and results for some of the studies are presented.

TSV Materials and Process Development

Many leading research institutes and semiconductor foundries are devoting their development efforts on TSV. Some sample research projects are described below.

Void-Free Bottom-up Via Filling Process

Peking University researchers have studies focused on TSV copper fill plating materials and process optimization using plating solutions provided from a local company, Shanghai Sinyang Corp. In one paper [6], they compared bath solutions with different levels of additives to examine the effects of additives including suppressors, accelerators, and levelers. A numerical simulation model was employed to describe the "absorption" (note: should be adsorption) of the suppressor and accelerator behavior during the plating process. The experimental result of filled TSV cross-section using one sample bath solution is shown in Figure 2; and that using an optimized bath is given in Figure 3.

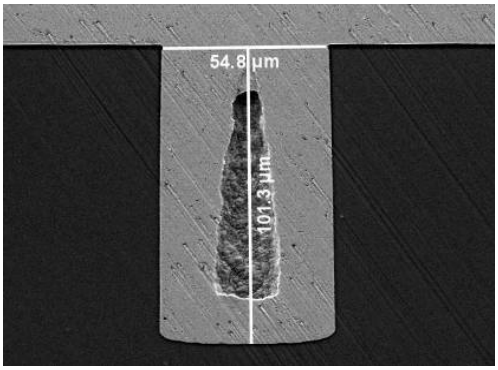

Figure 2. TSV Fill with Solution A

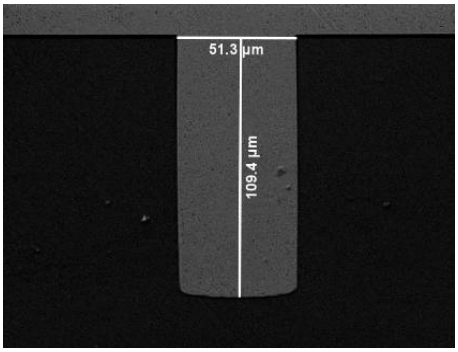

Figure 3. TSV Fill with Solution B

Low-cost TSV for MEMS Application

A rising star in MEMS and optoelectronics research, Huazhong University (Wuhan) published quite a few papers on TSV, particularly low cost process for use in 4-in wafers used in MEMS packaging. In one example [7], TSV having 60 µm size diameters are made by DRIE in 4-

inch wafers that are 370 µm thick, as shown in Figure 4. After bottom-up copper plating (Figure 5) showing cross-section), the wafer was sealed to a Pyrex7740 glass plate by anodic bonding; no CMP process was employed prior to the bonding to save cost. The authors claim that as long as the protruded caps on the top of TSV are less than 100 µm in height, the bonding results remained satisfactory.

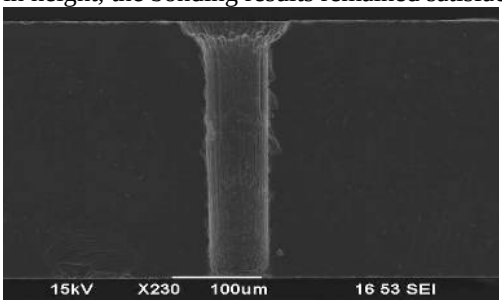

Figure 4. DRIE etched TSV

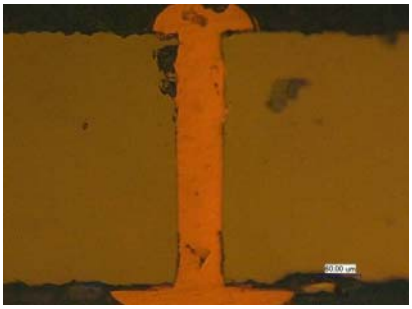

Figure 5. TSV after Bottom-up Copper Fill

Thermal Modeling of TSV in Package

Another Xidian University research paper [8] compared thermal distribution inside a package with TSV interposer underneath a power chip and compared that for a wire bonded package. There is a slight lowering in the temperature distribution. The study also found that the density of TSV (i.e., smaller pitches) would influence the thermal distribution. Figures 6 and 7 show the modeling analysis results for the TSV package and a conventional wire bond package, respectively.

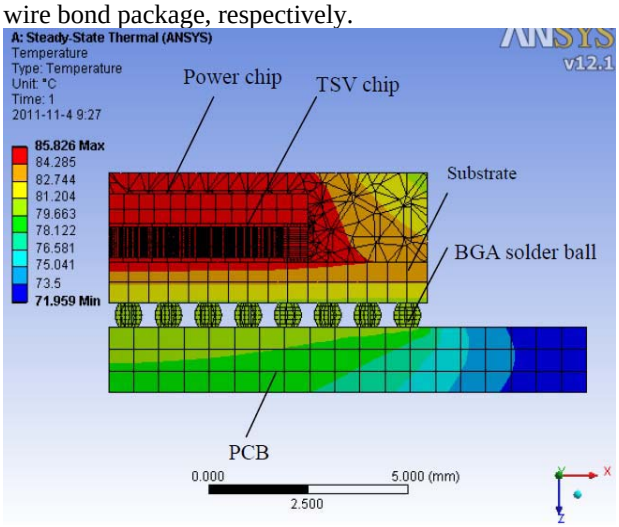

Figure 6. Temperature Distribution in a TSV substrate Package

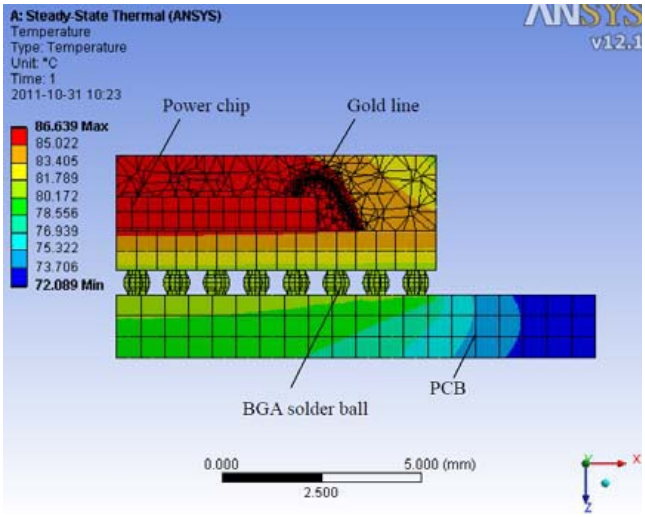

Figure 7. Temperature Distribution in a Wire Bond Package

Wafer Thinning-CMP Process

Tsinghua University presented a compressive review of the CMP process (Figure 8) and slurry application [9]. Using DOE studies of different slurry compositions, they found that higher peroxide concentration slurries should be used for wafers with thicker surface copper, due to accelerated CMP rates. The optimized slurry also resulted in very uniform wafer thickness, as shown in Figure 9, four different areas of a 50 um thinned wafer all measured to have a thickness of 48um, with the surface uniformity of less than 16nm RMS obtained.

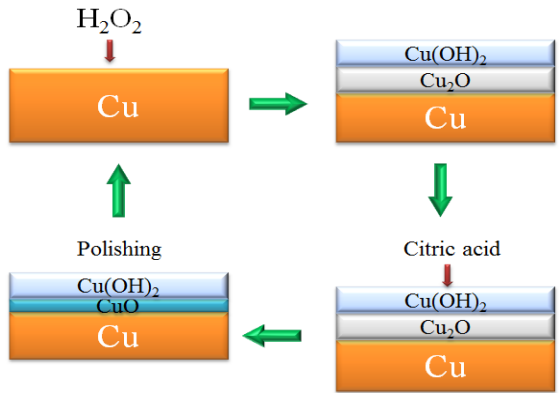

Figure 8. Peroxide based Slurry for CMP Process

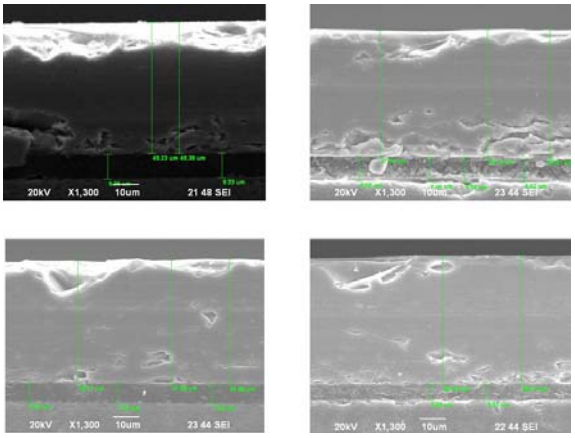

Figure 9. Thickness Measurement of Four Different areas in a 50um thinned Wafer

Low Temperature Wafer to Wafer Bonding

For applications in MEMS, this Peking University investigation [10] used two 4-in. silicon wafers with sputter coated Sn/Al surface, each 500 nm thick. The bonding conditions employed low temperature (280ºC), low pressure (0.25MPa), and short duration (3 minutes) in vacuum. After bonding, diced chips (10 mm x 5 mm) are examined for bond integrity and strength. Shear strengths between 3.1 and 5.7MPa are found. Figure 10 illustrates SEM images of fractured bond metal on the wafer surface after shearing.

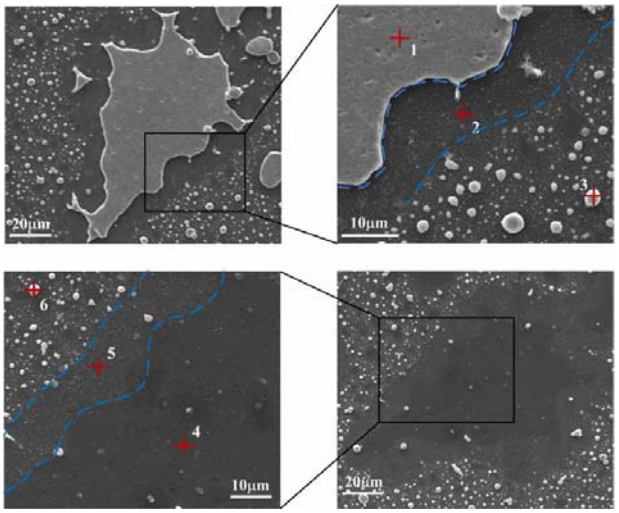

Figure 10. SEM Images of Fractured Metal Surfaces between top and bottom wafer after Shearing

INTERPOSER AND 2.5D INTEGRATION

In the package structure shown in Figure 11 by SIMIT-CAS, a silicon TSV interposer is bonded to a Si chip using indium micrbumps [11]. While fabricating the high-aspect ratio interposer with TSV, a supporting Si carrier must first be bonded to the bottom side of the interposer to form the bottom seed layer for subsequent bottom-up copper filling of the TSV. An Au-to-Au wafer level diffusion bonding process is applied as illustrated in Figure 12. With a 300ºC bonding temperature, the two separate gold surface coatings formed a join layer after solid state diffusion and remain electrically conductive. When the bonding temperature is increased to 400ºC, however, some Si and SiO_2 may diffuse into the gold layer, forming an Au/Si eutectic alloy layer that is unsuitable to use as the conductive seed layer for copper electroplating in the TSV.

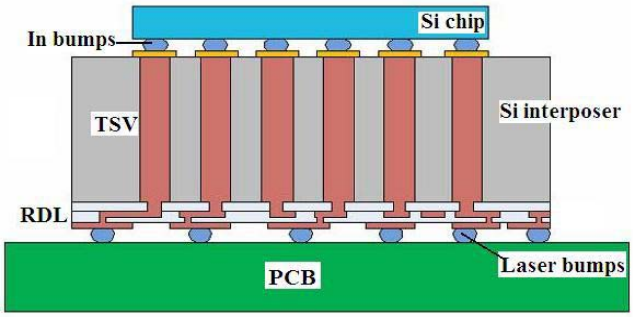

Figure 11. SIMIT-CAS 3D TSV Interposer

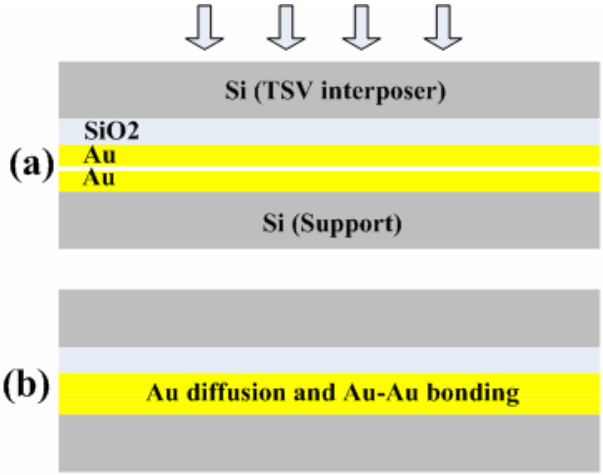

Figure 12. Au-to-Au Diffusion Bonding

Huawei 2.5D Packaging

Recently, Huawei announced an ambitious program with Altera to make 2.5 D interposer for integrating FPGA and wide I/O memory for networking applications [12]. Jiangyin Changdian Advanced Packaging Co. (JCAP) in Jiangsu province, who may be a partner of Huawei, announced an agreement recently signed with Singapore A*Star IME on jointly developing through silicon interposer (TSI) technology [13]. Figure 13 is an IME slide showing its 2.5D approach.

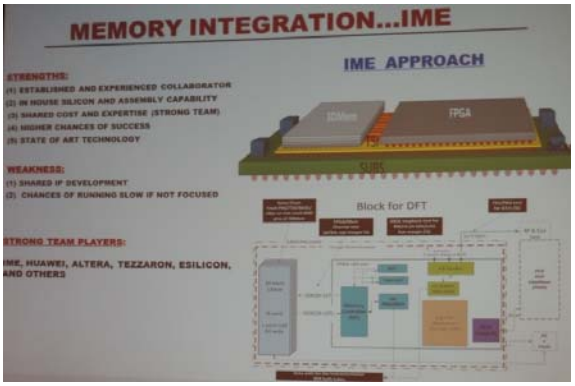

Figure 13. IME TSI 2.5D Package Concept

FOUNDRY EFFORTS

SMIC is also active in 3D IC, it formed a TSV technology department and its SVP, Dr ShiuhWuu Lee, presented a talk called "SMIC's Perspectives, Current Activities and High level plan on 2.5D/3D IC" at the 2012 SEMICON China 3DIC Technology Forum in March, 2012.

The upcoming SEMICON China 2013 (March 19, 2013, Shanghai) will have a 3D IC technology forum session, topics of interest include 3D IC design and manufacturing, EDA design tools, and IC manufacturing technology for telecom and wireless applications.

CONCLUSIONS

A multi-pronged progress in 3D IC integration research has been made by several leading research institutes and companies such as Huawei and JCAP within just a few years. Many applications are aimed at using 4 and 6-in size wafers, where wafer thinning, bonding and TSV fabrication are relatively easier compared to that for 300mm wafers. The near term fruit and resulting strength in China's efforts will be in practical, low-cost applications for camera modules, sensors, and MEMS. Some companies (Huawei, SMIC) are also planning to move into more complex interposers and 2.5D integration applications. In China, there are still plenty of market opportunities and growth potentials for mobile and computing devices to adopt 3D IC integration technologies for eventual high volume manufacturing in the coming years.

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